```
Parsing territory line UK
territory is UK
1 territory detected in the territories list.
Country UK has a code of 1
Numeric territory string is 01
Using module database 'HostFS::HardDisc4.$.Build.temp.OMAP3Dev.BuildSys.ModuleDB'.
Using components file
'HostFS::HardDisc4.$.Build.temp.OMAP3Dev.BuildSys.Components.ROOL.OMAP3'.
Using shadow components file
'HostFS::HardDisc4.$.Build.temp.OMAP3Dev.BuildSys.Shadow.ROOL.OMAP3'.
Set Locale (UK) and Resource$Dir to
HostFS::HardDisc4.$.Build.temp.OMAP3Dev.castle.RiscOS.Sources.Internat.Messages.Resources.
ROOL.OMAP3.01.UK
Opening log file 'HostFS::HardDisc4.$.Build.temp.OMAP3Dev.BuildSys.Logs.bUI800-00'.
--------------------------------------------------------------------------------
Started ROOL.OMAP3 build : Wed Sep 14 20:02:30 2011
Log filename       : bUI800-00
Image filename     : bUI800-00
Messages location  : castle.RiscOS.Sources.Internat.Messages
Image size         : 4096K
Joiner application : romlinker
Joiner format      : romlinker
--------------------------------------------------------------------------------
Starting phase rom ...

HAL_OMAP3 (castle.RiscOS.Sources.HAL.OMAP3)...
amu -E  -k rom COMPONENT=HAL_OMAP3 TARGET=OMAP3
AMU: in makefile included from Makefile (line 37):
AMU: in makefile Makefiles:CModule (line 191):
AMU: Re-inclusion of Makefiles:StdRules
OMAP-3 HAL: rom module built

Kernel (castle.RiscOS.Sources.Kernel)...
amu -E  -k rom COMPONENT=Kernel TARGET=Kernel
Kernel: rom module built

PCI (castle.RiscOS.Sources.HWSupport.PCI)...
amu -E  -k rom COMPONENT=PCI TARGET=PCI
PCI: rom module built

FileSwitch (castle.RiscOS.Sources.FileSys.FileSwitch)...
amu -E  -k rom COMPONENT=FileSwitch TARGET=FileSwitch
FileSwitch: rom module built

ResourceFS (castle.RiscOS.Sources.FileSys.ResourceFS.ResourceFS)...
amu -E  -k rom COMPONENT=ResourceFS TARGET=ResourceFS
ResourceFS: rom module built

TerritoryManager (castle.RiscOS.Sources.Internat.Territory.Manager)...
amu -E  -k rom COMPONENT=TerritoryManager TARGET=TerrMgr
TerritoryManager: rom module built

Messages (castle.RiscOS.Sources.Internat.Messages)...
amu -E  -k rom COMPONENT=Messages TARGET=Messages
Utils.ScanRes Processed.ROOL.OMAP3.<Build$LocaleListNumeric> Data.ROOL.OMAP3.<Build
$LocaleListNumeric>.Data
Scanning from directory Processed.ROOL.OMAP3.<Build$LocaleListNumeric>
Directory is
HostFS::HardDisc4.$.Build.temp.OMAP3Dev.castle.RiscOS.Sources.Internat.Messages.Processed.
ROOL.OMAP3.01.Common
```

```
Country code for Common is 0
Directory 0 is Common (territory numbers: 0 )
Appending data for territory resource dir
HostFS::HardDisc4.$.Build.temp.OMAP3Dev.castle.RiscOS.Sources.Internat.Messages.Processed.
ROOL.OMAP3.01.Common
set resdata Data.ROOL.OMAP3.<Build$LocaleListNumeric>.Data
objasm -Stamp -quit -depend !Depend    -ihdr -i<Hdr$Dir>.Global -i<Hdr$Dir>.Interface -
i<Hdr$Dir>.Interface2 -pd "APCS SETS \"APCS-32\"" -pd "Machine SETS \"CortexA8\"" -pd
"UserIF SETS \"Iyonix\"" -o o.Messages s.Messages
ARM AOF Macro Assembler 3.32 (Acorn Computers Ltd) [20 May 2010]
Unrecognised APCS qualifier /fpe3
Target cpu not recognised
link  -o rm.ROOL.OMAP3.<Build$LocaleListNumeric>.Messages -rmf o.Messages
unset resdata
Messages: rom module built for Build: ROOL.OMAP3.01

MessageTrans (castle.RiscOS.Sources.Internat.MsgTrans)...
amu -E  -k rom COMPONENT=MessageTrans TARGET=MsgTrans
MessageTrans: rom module built

UK (castle.RiscOS.Sources.Internat.Territory.Module)...
amu -E  -k rom COMPONENT=UK TARGET=UK
UK: rom module built

WindowManager (castle.RiscOS.Sources.Desktop.Wimp)...
amu -E  -k rom COMPONENT=WindowManager TARGET=Wimp OPTIONS=Ursula
do mkdir -p o.CortexA8
objasm -NoWarn -PreDefine "Options SETS \"Ursula\"" -Stamp -quit -depend !Depend    -ihdr
-i<Hdr$Dir>.Global -i<Hdr$Dir>.Interface -i<Hdr$Dir>.Interface2 -pd "APCS SETS
\"APCS-32\"" -pd "Machine SETS \"CortexA8\"" -pd "UserIF SETS \"Iyonix\"" -o
o.CortexA8.Wimp s.Wimp
ARM AOF Macro Assembler 3.32 (Acorn Computers Ltd) [20 May 2010]
Unrecognised APCS qualifier /fpe3
Target cpu not recognised
Error: Unknown opcode at line 1109 in file s.Wimp07
 included by GET/INCLUDE directive at line 103 in file "s.Wimp"
 1109 00014a48         WFSEQ   R5
Error: Unknown opcode at line 1115 in file s.Wimp07
 included by GET/INCLUDE directive at line 103 in file "s.Wimp"
 1115 00014a50         WFS     R5                      ; will still occur if FPEmulator
RMKilled
Error: Unknown opcode at line 1137 in file s.Wimp07
 included by GET/INCLUDE directive at line 103 in file "s.Wimp"
 1137 00014a5c         WFS     R5
Error: Unknown opcode at line 1367 in file s.Wimp07
 included by GET/INCLUDE directive at line 103 in file "s.Wimp"
 1367 00014bb0         RFS     R1                      ; <==== NB: pending trap can occur
here
Error: Unknown opcode at line 1383 in file s.Wimp07
 included by GET/INCLUDE directive at line 103 in file "s.Wimp"
 1383 00014bd8         WFS     R1
Assembly terminated:
5 Errors, 67 Warnings suppressed by -NOWarn
AMU: *** exit (1) ***


Desktop (castle.RiscOS.Sources.Desktop.Desktop)...
amu -E  -k rom COMPONENT=Desktop TARGET=Desktop
Desktop: rom module built
```

```
SharedRISC_OSLib (castle.RiscOS.Sources.Lib.RISC_OSLib)...
amu -E  -k rom COMPONENT=SharedRISC_OSLib TARGET=RISC_OSLib
objasm -PD "UROM SETL {TRUE}" rlib.s.poll rm_o_rl.poll -depend !Depend
ARM AOF Macro Assembler 3.32 (Acorn Computers Ltd) [20 May 2010]
Unrecognised APCS qualifier /fpe3
Target cpu not recognised
Error: Unknown opcode at line 116 in file rlib.s.poll
  116 000000b0         RFS     a2                      ; read FP status
Error: Unknown opcode at line 119 in file rlib.s.poll
  119 000000b8         WFS     a2
Error: Unknown opcode at line 121 in file rlib.s.poll
  121 000000bc         STFE    f4, [sp, #0*12]
Error: Unknown opcode at line 122 in file rlib.s.poll
  122 000000bc         STFE    f5, [sp, #1*12]
Error: Unknown opcode at line 123 in file rlib.s.poll
  123 000000bc         STFE    f6, [sp, #2*12]
Error: Unknown opcode at line 124 in file rlib.s.poll
  124 000000bc         STFE    f7, [sp, #3*12]
Error: Unknown opcode at line 130 in file rlib.s.poll
  130 000000c4         WFS     v1
Error: Unknown opcode at line 131 in file rlib.s.poll
  131 000000c4         LDFE    f4, [sp, #0*12]
Error: Unknown opcode at line 132 in file rlib.s.poll
  132 000000c4         LDFE    f5, [sp, #1*12]
Error: Unknown opcode at line 133 in file rlib.s.poll
  133 000000c4         LDFE    f6, [sp, #2*12]
Error: Unknown opcode at line 134 in file rlib.s.poll
  134 000000c4         LDFE    f7, [sp, #3*12]
Error: Unknown opcode at line 137 in file rlib.s.poll
  137 000000cc         WFS     v1
Assembly terminated:
12 Errors, 0 Warnings
AMU: *** exit (1) ***

objasm -depend !Depend   s.fenv rm_o.fenv
ARM AOF Macro Assembler 3.32 (Acorn Computers Ltd) [20 May 2010]
Unrecognised APCS qualifier /fpe3
Target cpu not recognised
Error: Unknown opcode at line 40 in file s.fenv
   40 00000000         RFS     ip
Error: Unknown opcode at line 43 in file s.fenv
   43 00000008         WFS     ip
Error: Unknown opcode at line 49 in file s.fenv
   49 00000010         RFS     ip
Error: Unknown opcode at line 58 in file s.fenv
   58 00000024         RFS     ip
Error: Unknown opcode at line 64 in file s.fenv
   64 00000038         WFS     ip
Error: Unknown opcode at line 70 in file s.fenv
   70 00000040         RFS     ip
Error: Unknown opcode at line 87 in file s.fenv
   87 0000005c         RFS     ip
Error: Unknown opcode at line 93 in file s.fenv
   93 00000064         RFS     ip
Error: Unknown opcode at line 97 in file s.fenv
   97 00000070         WFS     ip
Error: Unknown opcode at line 106 in file s.fenv
  106 00000084         WFS     ip
Error: Unknown opcode at line 107 in file s.fenv
  107 00000084         RFS     a1
```

```
Error: Unknown opcode at line 117 in file s.fenv
  117 0000009c         RFS     a4                      ; read current status
Error: Unknown opcode at line 118 in file s.fenv
  118 0000009c         WFS     ip                      ; write new status
Error: Unknown opcode at line 119 in file s.fenv
  119 0000009c         RFS     a3                      ; check we wrote it successfully
Error: Unknown opcode at line 131 in file s.fenv
  131 000000b0         MVFNES  f0, #0
Error: Unknown opcode at line 132 in file s.fenv
  132 000000b0         DVFNES  f0, f0, #0
Error: Unknown opcode at line 134 in file s.fenv
  134 000000b4         MVFNES  f0, #1
Error: Unknown opcode at line 135 in file s.fenv
  135 000000b4         DVFNES  f0, f0, #0
Error: Unknown opcode at line 137 in file s.fenv
  137 000000b8         LDFNES  f0, Huge
Error: Unknown opcode at line 138 in file s.fenv
  138 000000b8         MUFNES  f0, f0, #2              ; also generates inexact (allowed)
Error: Unknown opcode at line 141 in file s.fenv
  141 000000c0         LDFNES  f0, Tiny
Error: Unknown opcode at line 142 in file s.fenv
  142 000000c0         MUFNES  f0, f0, #0.5            ; also generates inexact (allowed)
Error: Unknown opcode at line 145 in file s.fenv
  145 000000c8         LDFNES  f0, TwoToTwentyEight
Error: Unknown opcode at line 146 in file s.fenv
  146 000000c8         ADFNES  f0, f0, #1
Assembly terminated:
24 Errors, 0 Warnings
AMU: *** exit (1) ***

objasm -depend !Depend   s.mathasm rm_o.mathasm
ARM AOF Macro Assembler 3.32 (Acorn Computers Ltd) [20 May 2010]
Unrecognised APCS qualifier /fpe3
Target cpu not recognised
Error: Unknown opcode at line 107 in file s.mathasm
  107 00000098         LDFD    f0,[sp],#8
Error: Unknown opcode at line 108 in file s.mathasm
  108 00000098         LDFD    f1,[sp],#8
Error: Unknown opcode at line 109 in file s.mathasm
  109 00000098         LDFD    f2,[sp,#0]
Error: Unknown opcode at line 116 in file s.mathasm
  116 0000009c         STFE    f2,[sp,#-12-8]!
Error: Unknown opcode at line 117 in file s.mathasm
  117 0000009c         STFE    f1,[sp,#-12]!
Error: Unknown opcode at line 118 in file s.mathasm
  118 0000009c         STFE    f0,[sp,#-12]!
Error: Unknown opcode at line 341 in file s.mathasm
  341 000002d4         LDFE    f0,[sp],#fma_framesize
Error: Unknown opcode at line 342 in file s.mathasm
  342 000002d4         MVFD    f0,f0
Error: Unknown opcode at line 357 in file s.mathasm
  357 000002e4         CMF     f2,#0
Error: Unknown opcode at line 358 in file s.mathasm
  358 000002e4         MVFVSD  f0,f2
Error: Unknown opcode at line 364 in file s.mathasm
  364 000002e4         MUFD    f0,f0,f1
Error: Unknown opcode at line 365 in file s.mathasm
  365 000002e4         ADFD    f0,f0,f2
Error: Unknown opcode at line 372 in file s.mathasm
  372 000002ec         MVFD    f0,f2
```

```
Error: Unknown opcode at line 383 in file s.mathasm
  383 000002f8         LDFD    f0, [sp], #8
Error: Unknown opcode at line 384 in file s.mathasm
  384 000002f8         LDFD    f1, [sp], #8
Error: Unknown opcode at line 385 in file s.mathasm
  385 000002f8         LDFD    f2, [sp, #0]
Error: Unknown opcode at line 387 in file s.mathasm
  387 000002f8         MVFS    f0, f0
Error: Unknown opcode at line 388 in file s.mathasm
  388 000002f8         MVFS    f1, f1
Error: Unknown opcode at line 389 in file s.mathasm
  389 000002f8         MVFS    f2, f2
Error: Unknown opcode at line 390 in file s.mathasm
  390 000002f8         FMLE    f0, f0, f1              ; IVO possible
Error: Unknown opcode at line 391 in file s.mathasm
  391 000002f8         ADFS    f0, f0, f2              ; UFL, OFL, INX possible
Error: Unknown opcode at line 404 in file s.mathasm
  404 00000300         LDFD    f0, [sp], #8
Error: Unknown opcode at line 406 in file s.mathasm
  406 00000300         CNF     f0, #0.5
Error: Unknown opcode at line 408 in file s.mathasm
  408 00000304         ADFE    f1, f0, #1              ; if (1+x) == 1, return x
Error: Unknown opcode at line 409 in file s.mathasm
  409 00000304         CMF     f1, #1                  ; gets INX right
Error: Unknown opcode at line 411 in file s.mathasm
  411 00000308         CMF     f0, #0.5
Error: Unknown opcode at line 413 in file s.mathasm
  413 0000030c         LGNE    f2, f1
Error: Unknown opcode at line 414 in file s.mathasm
  414 0000030c         MUFE    f2, f2, f0
Error: Unknown opcode at line 415 in file s.mathasm
  415 0000030c         SUFE    f3, f1, #1
Error: Unknown opcode at line 416 in file s.mathasm
  416 0000030c         DVFD    f0, f2, f3
Error: Unknown opcode at line 420 in file s.mathasm
  420 00000310         CNF     f0, #1                  ; To avoid inexact
Error: Unknown opcode at line 421 in file s.mathasm
  421 00000310         ADFGEE  f0, f0, #1
Error: Unknown opcode at line 422 in file s.mathasm
  422 00000310         LGND    f0, f0
Error: Unknown opcode at line 426 in file s.mathasm
  426 00000314         LGND    f0, f1
Error: Unknown opcode at line 432 in file s.mathasm
  432 0000031c         LDFD    f0, [sp], #8
Error: Unknown opcode at line 434 in file s.mathasm
  434 0000031c         MVFS    f0, f0
Error: Unknown opcode at line 435 in file s.mathasm
  435 0000031c         CNF     f0, #0.5
Error: Unknown opcode at line 437 in file s.mathasm
  437 00000320         ADFE    f1, f0, #1              ; if (1+x) == 1, return x
Error: Unknown opcode at line 438 in file s.mathasm
  438 00000320         CMF     f1, #1                  ; gets INX right
Error: Unknown opcode at line 440 in file s.mathasm
  440 00000324         CMF     f0, #0.5
Error: Unknown opcode at line 442 in file s.mathasm
  442 00000328         LGNE    f2, f1
Error: Unknown opcode at line 443 in file s.mathasm
  443 00000328         MUFE    f2, f2, f0
Error: Unknown opcode at line 444 in file s.mathasm
  444 00000328         SUFE    f3, f1, #1
```

```
Error: Unknown opcode at line 445 in file s.mathasm
  445 00000328         DVFS    f0, f2, f3
Error: Unknown opcode at line 449 in file s.mathasm
  449 0000032c         CNF     f0, #1                  ; To avoid inexact
Error: Unknown opcode at line 450 in file s.mathasm
  450 0000032c         ADFGEE  f0, f0, #1
Error: Unknown opcode at line 451 in file s.mathasm
  451 0000032c         LGND    f0, f0
Error: Unknown opcode at line 455 in file s.mathasm
  455 00000330         LGNS    f0, f1
Error: Unknown opcode at line 463 in macro Atan2
 at line 505 in file s.mathasm
  463 00000338         LDFD    f0, [sp], #8
Error: Unknown opcode at line 464 in macro Atan2
 at line 505 in file s.mathasm
  464 00000338         LDFD    f1, [sp], #8
Error: Unknown opcode at line 471 in macro Atan2
 at line 505 in file s.mathasm
  471 00000338         CMF     f0, f1
Assembly terminated:
51 Errors, 0 Warnings
AMU: *** exit (8) ***

objasm -depend !Depend   s.longlong rm_o.longlong
ARM AOF Macro Assembler 3.32 (Acorn Computers Ltd) [20 May 2010]
Unrecognised APCS qualifier /fpe3
Target cpu not recognised
Warning: Instruction not supported on targeted CPU at line 93 in file s.longlong
   93 00000008         MRC     cp15, 0, lr, c0, c0, 0
Warning: Instruction not supported on targeted CPU at line 106 in file s.longlong
  106 0000002c         MSRVS   CPSR_c, #0
Warning: Instruction not supported on targeted CPU at line 295 in file s.longlong
  295 00000128         UMULL   a1, lr, a3, a1
Warning: Instruction not supported on targeted CPU at line 296 in file s.longlong
  296 0000012c         MLA     lr, ip, a4, lr
Warning: Instruction not supported on targeted CPU at line 297 in file s.longlong
  297 00000130         MLA     a2, a3, a2, lr
Warning: Instruction not supported on targeted CPU at line 311 in file s.longlong
  311 00000138         MUL     a2, a3, a2          ; msw starts as aaaaaaaa * eeeeffff
Warning: Instruction not supported on targeted CPU at line 312 in file s.longlong
  312 0000013c         MLA     a2, a4, a1, a2      ; msw += dddddddd * bbbbcccc
Warning: Instruction not supported on targeted CPU at line 318 in file s.longlong
  318 00000150         MUL     a1, a3, a4          ; lsw starts as cccc * ffff
Warning: Instruction not supported on targeted CPU at line 320 in file s.longlong
  320 00000154         MUL     a4, ip, a4
Warning: Instruction not supported on targeted CPU at line 321 in file s.longlong
  321 00000158         MUL     a3, lr, a3
Warning: Instruction not supported on targeted CPU at line 327 in file s.longlong
  327 0000016c         MLA     a2, ip, lr, a2      ; msw completed by adding bbbb * eeee
Warning: Instruction not supported on targeted CPU at line 340 in file s.longlong
  340 00000188         UMULL   a1, lr, a3, a1
Warning: Instruction not supported on targeted CPU at line 341 in file s.longlong
  341 0000018c         MLA     a2, a3, a2, lr
Warning: Instruction not supported on targeted CPU at line 361 in file s.longlong
  361 000001b0         UMULL   a1, a2, lr, a2
Warning: Instruction not supported on targeted CPU at line 379 in file s.longlong
  379 000001dc         SMULL   a1, a2, lr, a2
Warning: Instruction not supported on targeted CPU at line 400 in file s.longlong
  400 00000218         MLAS    a1, a2, a1, a2
Warning: Instruction not supported on targeted CPU at line 432 in file s.longlong
```

```
  432 0000025c         CLZCS   a1, v6
Warning: Instruction not supported on targeted CPU at line 458 in file s.longlong
  458 000002b4         CLZCS   a1, v5
Warning: Instruction not supported on targeted CPU at line 497 in file s.longlong
  497 00000310         UMULL   a3, ip, v3, a1
Warning: Instruction not supported on targeted CPU at line 498 in file s.longlong
  498 00000314         UMULL   a4, lr, v4, a1
Warning: Instruction not supported on targeted CPU at line 515 in file s.longlong
  515 00000334         MUL     ip, a1, ip
Warning: Instruction not supported on targeted CPU at line 516 in file s.longlong
  516 00000338         MUL     fp, a1, fp
Warning: Instruction not supported on targeted CPU at line 517 in file s.longlong
  517 0000033c         MUL     a4, a1, a4
Warning: Instruction not supported on targeted CPU at line 518 in file s.longlong
  518 00000340         MUL     a3, a1, a3
Warning: Instruction not supported on targeted CPU at line 558 in file s.longlong
  558 000003b0         UMULLCS a3, ip, v5, lr
Warning: Instruction not supported on targeted CPU at line 559 in file s.longlong
  559 000003b4         MLACS   a4, v5, a4, ip
Warning: Instruction not supported on targeted CPU at line 560 in file s.longlong
  560 000003b8         MLACS   a4, v6, lr, a4
Warning: Instruction not supported on targeted CPU at line 565 in file s.longlong
  565 000003c0         MUL     a4, v5, a4
Warning: Instruction not supported on targeted CPU at line 566 in file s.longlong
  566 000003c4         MLA     a4, v6, a3, a4
Warning: Instruction not supported on targeted CPU at line 572 in file s.longlong
  572 000003d8         MUL     a3, fp, lr
Warning: Instruction not supported on targeted CPU at line 575 in file s.longlong
  575 000003e0         MUL     ip, lr, ip
Warning: Instruction not supported on targeted CPU at line 577 in file s.longlong
  577 000003e8         MUL     fp, lr, fp
Warning: Instruction not supported on targeted CPU at line 584 in file s.longlong
  584 00000400         MLA     a4, ip, lr, a4
Warning: Instruction not supported on targeted CPU at line 638 in file s.longlong
  638 00000470         UMULL   a4, a3, a1, ip
Warning: Instruction not supported on targeted CPU at line 639 in file s.longlong
  639 00000474         UMULL   a4, ip, a2, ip
Warning: Instruction not supported on targeted CPU at line 654 in file s.longlong
  654 000004a4         MUL     a3, a1, ip ; quotient * 10 (MSW is unimportant)
Warning: Instruction not supported on targeted CPU at line 660 in file s.longlong
  660 000004b4         MUL     a4, a3, a4
Warning: Instruction not supported on targeted CPU at line 664 in file s.longlong
  664 000004c4         MUL     a4, ip, a4
Warning: Instruction not supported on targeted CPU at line 679 in file s.longlong
  679 000004ec         MUL     a3, lr, a3          ; multiply through by &9999
Warning: Instruction not supported on targeted CPU at line 680 in file s.longlong
  680 000004f0         MUL     a4, lr, a4
Warning: Instruction not supported on targeted CPU at line 681 in file s.longlong
  681 000004f4         MUL     v1, lr, v1
Warning: Instruction not supported on targeted CPU at line 682 in file s.longlong
  682 000004f8         MUL     ip, lr, ip
Error: Unknown opcode at line 1385 in file s.longlong
 1385 00000d90         LDFD    f0,[sp],#8
Error: Unknown opcode at line 1386 in file s.longlong
 1386 00000d90         STFS    f0,[sp,#-4]!
Error: Unknown opcode at line 1394 in file s.longlong
 1394 00000e5c         LDFD    f0,[sp],#8
Error: Unknown opcode at line 1395 in file s.longlong
 1395 00000e5c         STFS    f0,[sp,#-4]!
Error: Unknown opcode at line 1415 in file s.longlong
```

```
 1415 00000f20         RFS     a2
Error: Unknown opcode at line 1424 in file s.longlong
 1424 00000f40         WFS     a2
Assembly terminated:
6 Errors, 42 Warnings
AMU: *** exit (1) ***

objasm -depend !Depend   s.cxsupport rm_o.cxsupport
ARM AOF Macro Assembler 3.32 (Acorn Computers Ltd) [20 May 2010]
Unrecognised APCS qualifier /fpe3
Target cpu not recognised
Error: Unknown opcode at line 59 in file s.cxsupport
   59 00000000         STFE    f0,[sp,#-12]!
Error: Unknown opcode at line 80 in file s.cxsupport
   80 00000044         STFE    f1,[sp,#-12]!
Error: Unknown opcode at line 81 in file s.cxsupport
   81 00000044         STFE    f0,[sp,#-12]!
Error: Unknown opcode at line 87 in file s.cxsupport
   87 00000058         LDFE    f0,[sp],#24
Error: Unknown opcode at line 92 in file s.cxsupport
   92 0000005c         MUFE    f0,f4,f6
Error: Unknown opcode at line 93 in file s.cxsupport
   93 0000005c         MUFE    f1,f5,f7
Error: Unknown opcode at line 94 in file s.cxsupport
   94 0000005c         SUFE    f0,f0,f1
Error: Unknown opcode at line 95 in file s.cxsupport
   95 0000005c         MUFE    f1,f5,f6
Error: Unknown opcode at line 96 in file s.cxsupport
   96 0000005c         MUFE    f2,f4,f7
Error: Unknown opcode at line 97 in file s.cxsupport
   97 0000005c         ADFE    f1,f1,f2
Error: Unknown opcode at line 98 in file s.cxsupport
   98 0000005c         CMF     f0,f0           ; if not (NaN+i*NaN) return now
Error: Unknown opcode at line 99 in file s.cxsupport
   99 0000005c         CMFVS   f1,f1
Error: Unknown opcode at line 106 in file s.cxsupport
  106 00000068         SFMFD   f0,2,[sp]!      ; remember original attempt
Error: Unknown opcode at line 108 in file s.cxsupport
  108 00000068         MVFE    f0,f4           ; v1-v4 = classification of f4-f7
Error: Unknown opcode at line 111 in file s.cxsupport
  111 00000070         MVFE    f0,f5
Error: Unknown opcode at line 114 in file s.cxsupport
  114 00000078         MVFE    f0,f6
Error: Unknown opcode at line 117 in file s.cxsupport
  117 00000080         MVFE    f0,f7
Error: Unknown opcode at line 127 in file s.cxsupport
  127 00000098         MVFEQE  f0,#1
Error: Unknown opcode at line 128 in file s.cxsupport
  128 00000098         MVFNEE  f0,#0
Error: Unknown opcode at line 129 in file s.cxsupport
  129 00000098         MVFE    f1,f4
Error: Unknown opcode at line 131 in file s.cxsupport
  131 0000009c         MVFE    f4,f0
Error: Unknown opcode at line 134 in file s.cxsupport
  134 000000a0         MVFEQE  f0,#1
Error: Unknown opcode at line 135 in file s.cxsupport
  135 000000a0         MVFNEE  f0,#0
Error: Unknown opcode at line 136 in file s.cxsupport
  136 000000a0         MVFE    f1,f5
Error: Unknown opcode at line 138 in file s.cxsupport
```

```
  138 000000a4         MVFE    f5,f0
Error: Unknown opcode at line 142 in file s.cxsupport
  142 000000ac         MVFE    f0,#0
Error: Unknown opcode at line 143 in file s.cxsupport
  143 000000ac         MVFE    f1,f6
Error: Unknown opcode at line 145 in file s.cxsupport
  145 000000b0         MVFE    f6,f0
Error: Unknown opcode at line 149 in file s.cxsupport
  149 000000b8         MVFE    f0,#0
Error: Unknown opcode at line 150 in file s.cxsupport
  150 000000b8         MVFE    f1,f7
Error: Unknown opcode at line 152 in file s.cxsupport
  152 000000bc         MVFE    f7,f0
Error: Unknown opcode at line 162 in file s.cxsupport
  162 000000d0         MVFEQE  f0,#1
Error: Unknown opcode at line 163 in file s.cxsupport
  163 000000d0         MVFNEE  f0,#0
Error: Unknown opcode at line 164 in file s.cxsupport
  164 000000d0         MVFE    f1,f6
Error: Unknown opcode at line 166 in file s.cxsupport
  166 000000d4         MVFE    f6,f0
Error: Unknown opcode at line 169 in file s.cxsupport
  169 000000d8         MVFEQE  f0,#1
Error: Unknown opcode at line 170 in file s.cxsupport
  170 000000d8         MVFNEE  f0,#0
Error: Unknown opcode at line 171 in file s.cxsupport
  171 000000d8         MVFE    f1,f7
Error: Unknown opcode at line 173 in file s.cxsupport
  173 000000dc         MVFE    f7,f0
Error: Unknown opcode at line 177 in file s.cxsupport
  177 000000e4         MVFE    f0,#0
Error: Unknown opcode at line 178 in file s.cxsupport
  178 000000e4         MVFE    f1,f4
Error: Unknown opcode at line 180 in file s.cxsupport
  180 000000e8         MVFE    f4,f0
Error: Unknown opcode at line 184 in file s.cxsupport
  184 000000f0         MVFE    f0,#0
Error: Unknown opcode at line 185 in file s.cxsupport
  185 000000f0         MVFE    f1,f5
Error: Unknown opcode at line 187 in file s.cxsupport
  187 000000f4         MVFE    f5,f0
Error: Unknown opcode at line 197 in file s.cxsupport
  197 000000fc         LFMNEFD f0,2,[sp]!
Error: Unknown opcode at line 200 in file s.cxsupport
  200 00000100         LDFE    f3,ExtInf
Error: Unknown opcode at line 201 in file s.cxsupport
  201 00000100         MUFE    f0,f4,f6
Error: Unknown opcode at line 202 in file s.cxsupport
  202 00000100         MUFE    f1,f5,f7
Error: Unknown opcode at line 203 in file s.cxsupport
  203 00000100         SUFE    f0,f0,f1
Error: Unknown opcode at line 204 in file s.cxsupport
  204 00000100         MUFE    f1,f5,f6
Assembly terminated:
51 Errors, 0 Warnings
AMU: *** exit (8) ***

objasm -depend !Depend   -PD "UROM SETL {TRUE}" -from clib.s.cl_mod_r -to rm_o.cl_modbody
ARM AOF Macro Assembler 3.32 (Acorn Computers Ltd) [20 May 2010]
Unrecognised APCS qualifier /fpe3
```

```
Target cpu not recognised
Warning: Instruction not supported on targeted CPU at line 399 in file clib.s.cl_body
  399 000007e4         MUL     a1, a2, a1
Error: Unknown opcode at line 609 in file clib.s.cl_body
  609 00000a5c         STFE    f7, [sp, #-12]!
Error: Unknown opcode at line 610 in file clib.s.cl_body
  610 00000a5c         STFE    f6, [sp, #-12]!
Error: Unknown opcode at line 611 in file clib.s.cl_body
  611 00000a5c         STFE    f5, [sp, #-12]!
Error: Unknown opcode at line 612 in file clib.s.cl_body
  612 00000a5c         STFE    f4, [sp, #-12]!
Warning: Instruction not supported on targeted CPU at line 474 in macro RemovePSRFromReg
 at line 633 in file clib.s.cl_body
  474 00000aa8         MRS     a2, CPSR
Warning: Instruction not supported on targeted CPU at line 701 in file clib.s.cl_body
  701 00000b3c         MRS     a4, CPSR
Error: Unknown opcode at line 749 in file clib.s.cl_body
  749 00000b60         SFMNE   f4, 4, [v1, #sj_f4]
Error: Unknown opcode at line 780 in file clib.s.cl_body
  780 00000ba4         LFMNE   f4, 4, [v1, #sj_f4-sj_f4]
Warning: Instruction not supported on targeted CPU at line 790 in file clib.s.cl_body
  790 00000bac         MRS     a1, CPSR
Error: Unknown opcode at line 59 in macro DisableFPInterrupts
 at line 881 in file clib.s.cl_body
   59 00000c88         RFS     ip
Error: Unknown opcode at line 60 in macro DisableFPInterrupts
 at line 881 in file clib.s.cl_body
   60 00000c88         WFS     r1
Error: Unknown opcode at line 882 in file clib.s.cl_body
  882 00000c88         LDFP    f0, [r0, #0]
Error: Unknown opcode at line 883 in file clib.s.cl_body
  883 00000c88         MVFD    f0, f0       ; (round to D format)
Error: Unknown opcode at line 75 in macro ReEnableFPInterrupts
 at line 884 in file clib.s.cl_body
   75 00000c88         RFS     r1
Error: Unknown opcode at line 77 in macro ReEnableFPInterrupts
 at line 884 in file clib.s.cl_body
   77 00000c88         WFS     ip
Error: Unknown opcode at line 895 in file clib.s.cl_body
  895 00000ca0         LDFD    f0, [sp], #8
Error: Unknown opcode at line 896 in file clib.s.cl_body
  896 00000ca0         STFP    f0, [r2, #0]
Error: Unknown opcode at line 913 in file clib.s.cl_body
  913 00000ca4         STFS    f0, [sp, #-4]!
Error: Unknown opcode at line 930 in file clib.s.cl_body
  930 00000cd8         STFD    f0, [sp, #-8]!
Error: Unknown opcode at line 948 in file clib.s.cl_body
  948 00000d10         STFS    f0, [sp, #-4]!
Error: Unknown opcode at line 954 in file clib.s.cl_body
  954 00000d1c         STFD    f0, [sp, #-8]!
Error: Unknown opcode at line 963 in file clib.s.cl_body
  963 00000d28         STFD    f1, [sp, #-8]!
Error: Unknown opcode at line 966 in file clib.s.cl_body
  966 00000d30         ABSD    f0, f0
Error: Unknown opcode at line 967 in file clib.s.cl_body
  967 00000d30         MNFMID  f0, f0
Error: Unknown opcode at line 974 in file clib.s.cl_body
  974 00000d34         STFS    f1, [sp, #-4]!
Error: Unknown opcode at line 977 in file clib.s.cl_body
  977 00000d3c         ABSS    f0, f0
```

```
Error: Unknown opcode at line 978 in file clib.s.cl_body
  978 00000d3c         MNFMIS  f0, f0
Error: Unknown opcode at line 988 in file clib.s.cl_body
  988 00000d4c         LDFD    f0, [sp], #8
Error: Unknown opcode at line 1000 in file clib.s.cl_body
 1000 00000d5c         LDFD    f0, [sp], #8
Error: Unknown opcode at line 1001 in file clib.s.cl_body
 1001 00000d5c         MVFS    f0, f0
Error: Unknown opcode at line 1010 in file clib.s.cl_body
 1010 00000d68         LDFD    f0, [sp], #8
Error: Unknown opcode at line 1011 in file clib.s.cl_body
 1011 00000d68         LDFD    f1, [sp], #8
Error: Unknown opcode at line 1013 in file clib.s.cl_body
 1013 00000d68         CMF     f1, f0
Error: Unknown opcode at line 1018 in file clib.s.cl_body
 1018 00000d74         ADFD    f0, f0, f1              ; do the NaN propagation +
exceptions
Error: Unknown opcode at line 1056 in file clib.s.cl_body
 1056 00000db4         LDFD    f0, [sp], #8
Error: Unknown opcode at line 1062 in file clib.s.cl_body
 1062 00000dc0         MUFS    f0,f0,#2                ; generate OVF+INX
Error: Unknown opcode at line 1073 in file clib.s.cl_body
 1073 00000dd0         LDFCSD  f0, [sp], #8
Error: Unknown opcode at line 1074 in file clib.s.cl_body
 1074 00000dd0         LDFCCD  f0, tiny_neg            ; +0 => smallest -ve subnormal
Error: Unknown opcode at line 1079 in file clib.s.cl_body
 1079 00000dd8         LDFD    f1,tiny_pos             ; generate UFL+INX
Error: Unknown opcode at line 1080 in file clib.s.cl_body
 1080 00000dd8         MUFD    f1,f1,#0.5
Error: Unknown opcode at line 1091 in file clib.s.cl_body
 1091 00000de8         LDFVCD  f0, [sp], #8
Error: Unknown opcode at line 1092 in file clib.s.cl_body
 1092 00000de8         LDFVSD  f0, tiny_pos            ; -0 => smallest +ve subnormal
Error: Unknown opcode at line 1100 in file clib.s.cl_body
 1100 00000df8         LDFD    f0, [sp], #8
Error: Unknown opcode at line 1101 in file clib.s.cl_body
 1101 00000df8         LDFD    f1, [sp], #8
Error: Unknown opcode at line 1103 in file clib.s.cl_body
 1103 00000df8         MVFS    f1, f1
Error: Unknown opcode at line 1111 in file clib.s.cl_body
 1111 00000e00         LDFD    f0, [sp], #8
Error: Unknown opcode at line 1112 in file clib.s.cl_body
 1112 00000e00         LDFD    f1, [sp], #8
Error: Unknown opcode at line 1115 in file clib.s.cl_body
 1115 00000e00         MVFS    f0, f0
Error: Unknown opcode at line 1116 in file clib.s.cl_body
 1116 00000e00         CMF     f1, f0
Error: Unknown opcode at line 1121 in file clib.s.cl_body
 1121 00000e0c         ADFS    f0, f0, f1              ; do the NaN propagation +
exceptions
Error: Unknown opcode at line 1125 in file clib.s.cl_body
 1125 00000e10         STFS    f0, [sp, #-4]!
Error: Unknown opcode at line 1132 in file clib.s.cl_body
 1132 00000e20         STFS    f0, [sp, #-4]!
Error: Unknown opcode at line 1153 in file clib.s.cl_body
 1153 00000e50         LDFS    f0, [sp], #4
Error: Unknown opcode at line 1165 in file clib.s.cl_body
 1165 00000e64         LDFCSS  f0, [sp], #4
Assembly terminated:
51 Errors, 4 Warnings
```

```
AMU: *** exit (8) ***

objasm -depend !Depend   -from kernel.s.k_mod_r -to rm_o.k_modbody
ARM AOF Macro Assembler 3.32 (Acorn Computers Ltd) [20 May 2010]
Unrecognised APCS qualifier /fpe3
Target cpu not recognised
Warning: Instruction not supported on targeted CPU at line 211 in file kernel.s.k_body
  211 000001bc         MRS     a1, CPSR
Warning: Instruction not supported on targeted CPU at line 270 in file kernel.s.k_body
  270 0000023c         MRS     ip, CPSR
Warning: Instruction not supported on targeted CPU at line 272 in file kernel.s.k_body
  272 00000244         MSR     CPSR_c, ip
Warning: Instruction not supported on targeted CPU at line 280 in file kernel.s.k_body
  280 0000024c         MRS     ip, CPSR
Warning: Instruction not supported on targeted CPU at line 282 in file kernel.s.k_body
  282 00000254         MSR     CPSR_c, ip
Warning: Instruction not supported on targeted CPU at line 292 in file kernel.s.k_body
  292 0000025c         MRS     a1, CPSR
Warning: Instruction not supported on targeted CPU at line 302 in file kernel.s.k_body
  302 00000274         MRS     ip, CPSR
Error: Unknown opcode at line 446 in file kernel.s.k_body
  446 00000408         WFSVC   r0
Warning: Instruction not supported on targeted CPU at line 585 in file kernel.s.k_body
  585 00000544         MRS     ip, CPSR
Warning: Instruction not supported on targeted CPU at line 671 in file kernel.s.k_body
  671 00000634         MRS     ip, CPSR
Warning: Instruction not supported on targeted CPU at line 843 in file kernel.s.k_body
  843 000007ec         MRSEQ   r3, CPSR
Warning: Instruction not supported on targeted CPU at line 846 in file kernel.s.k_body
  846 000007f8         MSREQ   CPSR_c, r0              ; if in 32-bit mode, probably ABT
Warning: Instruction not supported on targeted CPU at line 856 in file kernel.s.k_body
  856 00000810         MSREQ   CPSR_c, r3              ; back to original mode
Warning: Instruction not supported on targeted CPU at line 876 in file kernel.s.k_body
  876 00000840         MRSEQ   r1, SPSR                ; obtain aborter's mode from SPSR
Warning: Instruction not supported on targeted CPU at line 976 in file kernel.s.k_body
  976 00000948         MRSEQ   r3, CPSR
Warning: Instruction not supported on targeted CPU at line 979 in file kernel.s.k_body
  979 00000954         MRSEQ   r0, SPSR                ; obtain aborter's mode from SPSR
Warning: Instruction not supported on targeted CPU at line 988 in file kernel.s.k_body
  988 00000978         MSREQ   CPSR_c, #PSR32SVCMode+PSR32IBit+PSR32FBit
Warning: TSTP/TEQP/CMNP/CMPP inadvisable in 32-bit PC configurations at line 989 in file
kernel.s.k_body
  989 0000097c         TEQNEP  pc, #PSRSVCMode+PSRIBit+PSRFBit
Warning: Instruction not supported on targeted CPU at line 998 in file kernel.s.k_body
  998 000009a0         MSREQ   CPSR_cxs, r3
Warning: TSTP/TEQP/CMNP/CMPP inadvisable in 32-bit PC configurations at line 999 in file
kernel.s.k_body
  999 000009a4         TEQNEP  pc, r3
Warning: Instruction not supported on targeted CPU at line 1056 in file kernel.s.k_body
 1056 00000a2c         MRS     a1, CPSR
Warning: Instruction not supported on targeted CPU at line 1062 in file kernel.s.k_body
 1062 00000a38         MSR     CPSR_c, #PSR32IBit + PSR32USRMode       ; USR32, I set
Warning: Instruction not supported on targeted CPU at line 1064 in file kernel.s.k_body
 1064 00000a3c         MSR     CPSR_f, #PSRVBit                        ; set V for calling
IntOn.
Warning: TSTP/TEQP/CMNP/CMPP inadvisable in 32-bit PC configurations at line 1070 in file
kernel.s.k_body
 1070 00000a54         TEQP    a1, #0
Warning: Instruction not supported on targeted CPU at line 1254 in file kernel.s.k_body
 1254 00000ba4         MRS     v4, CPSR
```

```
Warning: Instruction not supported on targeted CPU at line 1586 in file kernel.s.k_body
 1586 00000f10         MRS     r14, CPSR
Warning: Instruction not supported on targeted CPU at line 1614 in file kernel.s.k_body
 1614 00000f44         SWPB    a1, a2, [a3]
Warning: Instruction not supported on targeted CPU at line 1689 in file kernel.s.k_body
 1689 00001010         MRS     r0, CPSR
Warning: Instruction not supported on targeted CPU at line 1785 in file kernel.s.k_body
 1785 00001120         MSRNE   CPSR_c, #PSR32IBit+PSR32SVCMode
Warning: Instruction not supported on targeted CPU at line 1786 in file kernel.s.k_body
 1786 00001124         MSREQ   CPSR_c, #PSR32IBit+PSRSVCMode
Warning: Instruction not supported on targeted CPU at line 1787 in file kernel.s.k_body
 1787 00001128         MSRNE   SPSR_cxsf, r1
Warning: Instruction not supported on targeted CPU at line 474 in macro RemovePSRFromReg
 at line 1835 in file kernel.s.k_body
  474 0000119c         MRS     lr, CPSR
Warning: Instruction not supported on targeted CPU at line 474 in macro RemovePSRFromReg
 at line 1845 in file kernel.s.k_body
  474 000011d0         MRS     lr, CPSR
Warning: Instruction not supported on targeted CPU at line 474 in macro RemovePSRFromReg
 at line 1866 in file kernel.s.k_body
  474 00001214         MRS     lr, CPSR
Warning: Instruction not supported on targeted CPU at line 474 in macro RemovePSRFromReg
 at line 1901 in file kernel.s.k_body
  474 00001278         MRS     v1, CPSR
Error: Unknown opcode at line 1970 in file kernel.s.k_body
 1970 00001358 15      LFM     f0, 1, [v2], #12
Error: Unknown opcode at line 1972 in file kernel.s.k_body
 1972 0000135c         STFE    f0, [v3], #12
Warning: Instruction not supported on targeted CPU at line 474 in macro RemovePSRFromReg
 at line 2007 in file kernel.s.k_body
  474 000013c8         MRS     v2, CPSR
Warning: Instruction not supported on targeted CPU at line 2021 in file kernel.s.k_body
 2021 00001404         MRS     r14, CPSR
Warning: Instruction not supported on targeted CPU at line 2024 in file kernel.s.k_body
 2024 00001410         MSRNE   CPSR_c, r14
Warning: TSTP/TEQP/CMNP/CMPP inadvisable in 32-bit PC configurations at line 2026 in file
kernel.s.k_body
 2026 00001418         TEQEQP  r14, #0                 ; Back to the mode and interrupt
Error: Unknown opcode at line 2216 in file kernel.s.k_body
 2216 0000163c         SFMNEFD f4, 4, [sp]!
Error: Unknown opcode at line 2217 in file kernel.s.k_body
 2217 0000163c         RFSNE   v5
Warning: Instruction not supported on targeted CPU at line 474 in macro RemovePSRFromReg
 at line 2273 in file kernel.s.k_body
  474 000016c4         MRS     v4, CPSR
Warning: Instruction not supported on targeted CPU at line 474 in macro RemovePSRFromReg
 at line 2367 in file kernel.s.k_body
  474 000017d0         MRS     v3, CPSR
Error: Unknown opcode at line 2404 in file kernel.s.k_body
 2404 00001850         WFSNE   v5
Error: Unknown opcode at line 2405 in file kernel.s.k_body
 2405 00001850         LFMNEFD f4, 4, [sp]!
Warning: Instruction not supported on targeted CPU at line 2868 in file kernel.s.k_body
 2868 00001c94         MRS     v2, CPSR
Warning: Instruction not supported on targeted CPU at line 2871 in file kernel.s.k_body
 2871 00001ca0         MSRNE   CPSR_f, #V_bit          ; maintain NE
Warning: Instruction not supported on targeted CPU at line 2909 in file kernel.s.k_body
 2909 00001d0c         SWP     a1, a1, [a2]
Warning: Instruction not supported on targeted CPU at line 2965 in file kernel.s.k_body
 2965 00001dc0         MSR     CPSR_f, #V_bit
```

```
Warning: Instruction not supported on targeted CPU at line 474 in macro RemovePSRFromReg
 at line 3195 in file kernel.s.k_body
  474 0000203c         MRS     r1, CPSR
Warning: Instruction not supported on targeted CPU at line 3410 in file kernel.s.k_body
 3410 00002200         MRS     a4, CPSR
Warning: Instruction not supported on targeted CPU at line 3428 in file kernel.s.k_body
 3428 00002238         MSR     CPSR_c, a4              ; Restore mode and IRQs
Assembly terminated:
7 Errors, 47 Warnings
AMU: *** exit (1) ***


OMAPVideo (bsd.RiscOS.Sources.Video.HWSupport.OMAPVideo)...
amu -E  -k rom COMPONENT=OMAPVideo TARGET=OMAPVideo DEBUG=TRUE
OMAPVideo: rom module built

TaskManager (castle.RiscOS.Sources.Desktop.Switcher)...
amu -E  -k rom COMPONENT=TaskManager TARGET=Switcher
TaskManager: rom module built

ARM (castle.RiscOS.Sources.HWSupport.ARM)...
amu -E  -k rom COMPONENT=ARM TARGET=ARM
ARM: rom module built

BASIC105 (castle.RiscOS.Sources.Programmer.BASIC)...
amu -E  -k rom COMPONENT=BASIC105 TARGET=BASIC105
BASIC105: rom module built

BASIC64 (castle.RiscOS.Sources.Programmer.BASIC)...
amu -E  -k rom COMPONENT=BASIC64 TARGET=BASIC64
do mkdir -p o.CortexA8
objasm -Stamp -quit -depend !Depend    -ihdr -i<Hdr$Dir>.Global -i<Hdr$Dir>.Interface -
i<Hdr$Dir>.Interface2 -pd "APCS SETS \"APCS-32\"" -pd "Machine SETS \"CortexA8\"" -pd
"UserIF SETS \"Iyonix\"" -o o.CortexA8.BASIC64 s.BASIC64
ARM AOF Macro Assembler 3.32 (Acorn Computers Ltd) [20 May 2010]
Unrecognised APCS qualifier /fpe3
Target cpu not recognised
Warning: Instruction not supported on targeted CPU at line 23 in file s.BASIC
   23 00000108         MRS     R1,CPSR
Warning: Instruction not supported on targeted CPU at line 25 in file s.BASIC
   25 00000110         MSR     CPSR_c,R1
Warning: Instruction not supported on targeted CPU at line 140 in file s.BASIC
  140 00000284         MRS     R3,CPSR
Warning: Instruction not supported on targeted CPU at line 142 in file s.BASIC
  142 0000028c         MSR     CPSR_c,R3               ; change down to user mode (is this
safe???)
Error: Unknown opcode at line 231 in file s.BASIC
  231 000003bc         WFS     R0
Error: Unknown opcode at line 667 in file s.BASIC
  667 00000bdc         RSFMID  FACC,FACC,#0
Error: Unknown opcode at line 743 in file s.BASIC
  743 00000cd4         LDFD    F1,[R4]
Error: Unknown opcode at line 744 in file s.BASIC
  744 00000cd4         ADFD    FACC,F1,FACC
Error: Unknown opcode at line 745 in file s.BASIC
  745 00000cd4         STFD    FACC,[R4]
Warning: Instruction not supported on targeted CPU at line 1144 in file s.BASIC
 1144 000012a4         MRS     R14,CPSR
Warning: Instruction not supported on targeted CPU at line 1178 in file s.BASIC
 1178 000012dc         MSR     CPSR_f,R14
```

```
Warning: Instruction not supported on targeted CPU at line 1195 in file s.BASIC
 1195 00001304         MSR     CPSR_f,R14
Error: Unknown opcode at line 50 in file s.Fp
   50 0000172c         FLTD    FACC,IACC
Error: Unknown opcode at line 60 in file s.Fp
   60 00001740         FIXZ    IACC,FACC
Error: Unknown opcode at line 919 in file s.Fp
  919 00001750         ASND    FACC,FACC
Error: Unknown opcode at line 923 in file s.Fp
  923 00001760 PI      LDFD    FACC,FULLPI
Error: Unknown opcode at line 47 in file s.Fp2
   47 00001774         COSD    FACC,FACC
Error: Unknown opcode at line 177 in file s.Fp2
  177 00001788         SIND    FACC,FACC
Error: Unknown opcode at line 269 in file s.Fp2
  269 0000179c         ATND    FACC,FACC
Error: Unknown opcode at line 559 in file s.Fp2
  559 000017fc         STFP    FACC,[SP,#-12]!
Error: Unknown opcode at line 936 in file s.Fp2
  936 00001b34         FLTE    FACC,IACC              ;mantissa now floated
Error: Unknown opcode at line 946 in file s.Fp2
  946 00001b58         MUFE    FACC,FACC,#10
Error: Unknown opcode at line 948 in file s.Fp2
  948 00001b5c         FLTE    F1,R10
Error: Unknown opcode at line 950 in file s.Fp2
  950 00001b60         ADFE    FACC,FACC,F1           ;mult by 10 and add next char
Error: Unknown opcode at line 957 in file s.Fp2
  957 00001b70         FLTE    FACC,IACC
Error: Unknown opcode at line 965 in file s.Fp2
  965 00001b8c FRDDP   MUFE    FACC,FACC,#10
Error: Unknown opcode at line 969 in file s.Fp2
  969 00001b98 FRDDM   DVFE    FACC,FACC,#10
Error: Unknown opcode at line 972 in file s.Fp2
  972 00001ba0 FRDDZ   MVFD    FACC,FACC
Warning: Instruction not supported on targeted CPU at line 530 in file s.Expr
  530 000023d4         MUL     R5,R6,IACC
Error: Unknown opcode at line 152 in macro FPUSH
 at line 595 in file s.Expr
  152 000024a0       STFD    FACC,[SP,#-8]!
Error: Unknown opcode at line 622 in file s.Expr
  622 000024e4         LDFD    FACC,[SP],#8
Error: Unknown opcode at line 717 in file s.Expr
  717 00002590         FLTD    F1,R4                  ;float first number
Error: Unknown opcode at line 152 in macro FPUSH
 at line 720 in file s.Expr
  152 00002598       STFD    FACC,[SP,#-8]!
Error: Unknown opcode at line 724 in file s.Expr
  724 000025a4         FLTPLD  FACC,IACC              ;float if rqd
Error: Unknown opcode at line 725 in file s.Expr
  725 000025a4         LDFD    F1,[SP],#8             ;get first
Error: Unknown opcode at line 727 in file s.Expr
  727 000025a8         CMF     F1,FACC
Error: Unknown opcode at line 152 in macro FPUSH
 at line 910 in file s.Expr
  152 00002824       STFD    FACC,[SP,#-8]!
Error: Unknown opcode at line 914 in file s.Expr
  914 00002830         FLTPLD  FACC,IACC
Error: Unknown opcode at line 915 in file s.Expr
  915 00002830         LDFD    F1,[SP],#8
Error: Unknown opcode at line 917 in file s.Expr
```

```
  917 00002834 FPLUSS  ADFD    FACC,FACC,F1
Error: Unknown opcode at line 941 in file s.Expr
  941 00002850         FLTD    F1,IACC                ;no need to change type
Error: Unknown opcode at line 944 in file s.Expr
  944 00002858         FLTD    F1,IACC
Error: Unknown opcode at line 945 in file s.Expr
  945 00002858         SUFD    FACC,F1,FACC
Error: Unknown opcode at line 152 in macro FPUSH
 at line 948 in file s.Expr
  152 00002860       STFD    FACC,[SP,#-8]!
Error: Unknown opcode at line 952 in file s.Expr
  952 0000286c         FLTPLD  FACC,IACC
Error: Unknown opcode at line 953 in file s.Expr
  953 0000286c         LDFD    F1,[SP],#8
Error: Unknown opcode at line 954 in file s.Expr
  954 0000286c         SUFD    FACC,F1,FACC
Warning: Instruction not supported on targeted CPU at line 986 in file s.Expr
  986 000028ec         MUL     IACC,R4,IACC
Error: Unknown opcode at line 1006 in file s.Expr
 1006 00002904 FTIMEL  FLTD    FACC,IACC
Error: Unknown opcode at line 1008 in file s.Expr
 1008 00002908         FLTD    F1,R4
Error: Unknown opcode at line 1010 in file s.Expr
 1010 0000290c FTIMF   FLTD    FACC,IACC
Error: Unknown opcode at line 152 in macro FPUSH
 at line 1012 in file s.Expr
  152 00002910       STFD    FACC,[SP,#-8]!
Error: Unknown opcode at line 1016 in file s.Expr
 1016 0000291c         FLTPLD  FACC,IACC
Error: Unknown opcode at line 1017 in file s.Expr
 1017 0000291c         LDFD    F1,[SP],#8
Error: Unknown opcode at line 1018 in file s.Expr
 1018 0000291c FTIMES  MUFD    FACC,F1,FACC
Error: Unknown opcode at line 152 in macro FPUSH
 at line 1039 in file s.Expr
  152 00002944       STFD    FACC,[SP,#-8]!
Error: Unknown opcode at line 1043 in file s.Expr
 1043 00002950         CMF     FACC,#0
Error: Unknown opcode at line 1045 in file s.Expr
 1045 00002954         LDFD    F1,[SP],#8
Error: Unknown opcode at line 1046 in file s.Expr
 1046 00002954         DVFD    FACC,F1,FACC
Error: Unknown opcode at line 152 in macro FPUSH
 at line 1170 in file s.Expr
  152 00002dcc       STFD    FACC,[SP,#-8]!
Assembly terminated:
51 Errors, 9 Warnings
AMU: *** exit (8) ***


BASICTrans (castle.RiscOS.Sources.Programmer.BASICTrans)...
amu -E  -k rom COMPONENT=BASICTrans TARGET=BASICTrans
BASICTrans: rom module built

BufferManager (castle.RiscOS.Sources.HWSupport.Buffers)...
amu -E  -k rom COMPONENT=BufferManager TARGET=Buffers
BufferManager: rom module built

ColourTrans (castle.RiscOS.Sources.Video.Render.Colours)...
amu -E  -k rom COMPONENT=ColourTrans TARGET=Colours
```

```
ColourTrans: rom module built

Debugger (castle.RiscOS.Sources.Programmer.Debugger)...
amu -E  -k rom COMPONENT=Debugger TARGET=Debugger
do mkdir -p o.CortexA8
objasm -Stamp -quit -depend !Depend    -ihdr -i<Hdr$Dir>.Global -i<Hdr$Dir>.Interface -
i<Hdr$Dir>.Interface2 -pd "APCS SETS \"APCS-32\"" -pd "Machine SETS \"CortexA8\"" -pd
"UserIF SETS \"Iyonix\"" -o o.CortexA8.Debugger s.Debugger
ARM AOF Macro Assembler 3.32 (Acorn Computers Ltd) [20 May 2010]
Unrecognised APCS qualifier /fpe3
Target cpu not recognised
Warning: Instruction not supported on targeted CPU at line 614 in file s.Debugger
  614 00000140         MRS     R3, CPSR
Warning: Instruction not supported on targeted CPU at line 3793 in file s.Debugger
 3793 00002034         LDRD    r2, [r0]         ;read to r2,r3
Warning: Instruction not supported on targeted CPU at line 3803 in file s.Debugger
 3803 00002058         LDRD    r0, [r2]         ;read from logical mapping into r0,r1
Warning: Instruction not supported on targeted CPU at line 3836 in file s.Debugger
 3836 000020c4         LDRH    r1, [r0]
Warning: Instruction not supported on targeted CPU at line 3844 in file s.Debugger
 3844 000020e0         LDRH    r2, [r2]         ;read from logical mapping
Warning: Instruction not supported on targeted CPU at line 3877 in file s.Debugger
 3877 0000214c         STRD    r2, [r0]         ;write from r2,r3
Warning: Instruction not supported on targeted CPU at line 3887 in file s.Debugger
 3887 00002170         STRD    r0, [r2]         ;store from r0,r1 into logical mapping
Warning: Instruction not supported on targeted CPU at line 3920 in file s.Debugger
 3920 000021dc         STRH    r1, [r0]
Warning: Instruction not supported on targeted CPU at line 3929 in file s.Debugger
 3929 000021fc         STRH    r1, [r2]         ;write to logical mapping
Warning: Instruction not supported on targeted CPU at line 3979 in file s.Debugger
 3979 00002284         MRC     p15,0,r0,c0,c0,0
Warning: Instruction not supported on targeted CPU at line 3987 in file s.Debugger
 3987 000022a4         MRC     p15, 0, r0, c1, c0, 0
Warning: TSTP/TEQP/CMNP/CMPP inadvisable in 32-bit PC configurations at line 5046 in file
s.Debugger
 5046 00002e34         TEQP    r14_svc, #F_bit + I_bit ; Enter correct mode, ints off
Warning: Instruction not supported on targeted CPU at line 5066 in file s.Debugger
 5066 00002e6c         MSR     CPSR_c, r1              ; Enter correct mode, ints off
Warning: Instruction not supported on targeted CPU at line 5067 in file s.Debugger
 5067 00002e70         MSR     SPSR_cxsf, r14_svc      ; Set up SPSR ready for return
Warning: Instruction not supported on targeted CPU at line 5071 in file s.Debugger
 5071 00002e78         MRS     r14_svc, CPSR
Warning: Instruction not supported on targeted CPU at line 5073 in file s.Debugger
 5073 00002e80         MSR     CPSR_c, r14_svc         ; IRQs off for SPSR use
Warning: Instruction not supported on targeted CPU at line 5076 in file s.Debugger
 5076 00002e88         MSR     SPSR_cxsf, r14_svc      ; Set up SPSR ready for return
Warning: Instruction not supported on targeted CPU at line 5382 in file s.Debugger
 5382 000031e4         MRS     r4, CPSR
Error: Unknown opcode at line 458 in file s.FP
  458 000039ac         RFS     r1                      ; save current FPSR
Error: Unknown opcode at line 461 in file s.FP
  461 000039b4         WFS     r1
Error: Unknown opcode at line 464 in file s.FP
  464 000039bc         SFM     f0, 1, [r4]             ; and save F0
Error: Unknown opcode at line 552 in file s.FP
  552 00003acc         LDFE    f0, [r11], #12          ; get extended value from dump
Error: Unknown opcode at line 555 in file s.FP
  555 00003ad4         STFP    f0, [r3]                ; and convert to packed decimal
Error: Unknown opcode at line 643 in file s.FP
  643 00003c00         LFM     f0, 1, [r1]
```

```
Error: Unknown opcode at line 646 in file s.FP
  646 00003c08         WFS     r1                      ; restore FPSR
Assembly terminated:
7 Errors, 18 Warnings
AMU: *** exit (1) ***


DeviceFS (castle.RiscOS.Sources.HWSupport.DeviceFS)...
amu -E  -k rom COMPONENT=DeviceFS TARGET=DeviceFS
DeviceFS: rom module built

PortableHAL (castle.RiscOS.Sources.HWSupport.PortableHAL)...
amu -E  -k rom COMPONENT=PortableHAL TARGET=Portable
Portable: rom module built

RTSupport (castle.RiscOS.Sources.Programmer.RTSupport)...
amu -E  -k rom COMPONENT=RTSupport TARGET=RTSupport
Real Time Support: rom module built

USBDriver (mixed.RiscOS.Sources.HWSupport.USB.NetBSD.build)...
amu -E  -k rom COMPONENT=USBDriver TARGET=USBDriver CFLAGS="-DRHENIUM " -DRHENIUM
CMHGFLAGS="-DRHENIUM "
aof.USBDriver does not yet exist
do mkdir -p aof
link -o aof.USBDriver -aof usbmodhead.o  usbmodule.o  port.o  usb.o  usbdi.o  usb_subr.o
usbdi_util.o  usb_quirks.o  uhub.o  usbmouse.o  usbkboard.o  hid.o  bufman.o  triggercbs.o
call_veneer.o C:DebugLib.o.DebugLibZM C:ModMalloc.o.Lib_M C:Wild.o.Wild_M
C:DDTLib.o.DDTLib_M C:Desk.o.Desk_M  TCPIPLibs:o.unixlibzm TCPIPLibs:o.inetlibzm
TCPIPLibs:o.socklib5zm C:callx.o.callx C:AsmUtils.o.AsmUtilsZM C:tboxlibs.o.eventlibm
C:tboxlibs.o.toolboxlib C:tboxlibs.o.renderlib C:tboxlibs.o.wimplib RISCOSLIB:o.romcstubs
ARM Linker: (Fatal) File C:AsmUtils.o.AsmUtilsZM not found.
AMU: *** exit (1) ***


EHCIDriver (mixed.RiscOS.Sources.HWSupport.USB.NetBSD.build)...
amu -E  -k rom COMPONENT=EHCIDriver TARGET=EHCIDriver CFLAGS="-DRHENIUM " -DRHENIUM
CMHGFLAGS="-DRHENIUM "
h.USBDriver is out of date w.r.t. h.usbmodhead
sed -n "/define USBDriver_/p" h.usbmodhead > h.USBDriver
o.ehcimodule is out of date w.r.t. h.USBDriver
cc -DRHENIUM  -ff -wp -wc -zm -zps1 -c -depend !Depend   -DKERNEL -D_KERNEL -Dpaddr_t=int
-D__P(A)=A -DKLD_MODULE -DDISABLE_PACKED -Itbox:,TCPIPLibs:,^.,OS: -ff -fah -o
o.ehcimodule c.ehcimodule
Norcroft RISC OS ARM C vsn 5.69 [20 Oct 2010]
"c.ehcimodule", line 66: Warning: extern 'private_word' not declared in header
"c.ehcimodule", line 68: Warning: extern 'ehci_base' not declared in header
"c.ehcimodule", line 70: Warning: extern 'ehci_soft' not declared in header
"c.ehcimodule", line 71: Warning: extern 'usb_soft' not declared in header
"c.ehcimodule", line 106: Warning: extern 'magic' not declared in header
"c.ehcimodule", line 109: Warning: extern 'build_veneer' not declared in header
"c.ehcimodule", line 139: Warning: extern 'pci_device' not declared in header
"c.ehcimodule", line 140: Warning: extern 'instance' not declared in header
"c.ehcimodule", line 141: Warning: extern 'device_number' not declared in header
"c.ehcimodule", line 142: Warning: extern 'unhandled_irqs' not declared in header
"c.ehcimodule", line 145: Warning: extern 'registers_32bit' not declared in header
"c.ehcimodule", line 149: Warning: extern 'register_bus' not declared in header
"c.ehcimodule", line 165: Warning: extern 'new_instance' not declared in header
"c.ehcimodule", line 200: Warning: variable 'h' declared but not used
"c.ehcimodule", line 412: Warning: variable 'podule' declared but not used
"c.ehcimodule", line 412: Warning: variable 'fatal' declared but not used
```

```
"c.ehcimodule", line 459: Warning: variable 'pw' declared but not used
"c.ehcimodule", line 614: Warning: variable 'pw' declared but not used
"c.ehcimodule", line 614: Warning: variable 'r' declared but not used
"c.ehcimodule", line 623: Warning: variable 'ioh' declared but not used
"c.ehcimodule", line 623: Warning: variable 'iot' declared but not used
"c.ehcimodule", line 632: Warning: variable 'ioh' declared but not used
"c.ehcimodule", line 632: Warning: variable 'iot' declared but not used
"c.ehcimodule", line 652: Warning: variable 'ioh' declared but not used
"c.ehcimodule", line 652: Warning: variable 'iot' declared but not used
"c.ehcimodule", line 678: Warning: variable 'ioh' declared but not used
"c.ehcimodule", line 678: Warning: variable 'iot' declared but not used
"c.ehcimodule", line 698: Warning: variable 'ioh' declared but not used
"c.ehcimodule", line 698: Warning: variable 'iot' declared but not used
"c.ehcimodule", line 719: Warning: variable 'ioh' declared but not used
"c.ehcimodule", line 719: Warning: variable 'iot' declared but not used
"c.ehcimodule", line 725: Warning: variable 't' declared but not used
"c.ehcimodule", line 725: Warning: variable 'h' declared but not used
"c.ehcimodule", line 725: Warning: variable 'f' declared but not used
"c.ehcimodule", line 730: Warning: variable 'h' declared but not used
"c.ehcimodule", line 730: Warning: variable 'f' declared but not used
"c.ehcimodule", line 737: Warning: variable 'h' declared but not used
"c.ehcimodule", line 755: Warning: extern '_riscos_abort_pipe' not declared in header
"c.ehcimodule", line 758: Warning: variable 'pw' declared but not used
"c.ehcimodule", line 758: Warning: variable 'r' declared but not used
"c.ehcimodule", line 808: Warning: variable 'pw' declared but not used
c.ehcimodule: 41 warnings, 0 errors, 0 serious errors
aof.EHCIDriver does not yet exist
do mkdir -p aof
link -o aof.EHCIDriver -aof ehcimodhead.o    ehcimodule.o    ehci.o    port.o
call_veneer.o    triggercbs.o  usbroothub_subr.o C:DebugLib.o.DebugLibZM
C:ModMalloc.o.Lib_M C:Wild.o.Wild_M C:DDTLib.o.DDTLib_M C:Desk.o.Desk_M
TCPIPLibs:o.unixlibzm TCPIPLibs:o.inetlibzm TCPIPLibs:o.socklib5zm C:callx.o.callx
C:AsmUtils.o.AsmUtilsZM C:tboxlibs.o.eventlibm C:tboxlibs.o.toolboxlib
C:tboxlibs.o.renderlib C:tboxlibs.o.wimplib RISCOSLIB:o.romcstubs
ARM Linker: (Fatal) File C:AsmUtils.o.AsmUtilsZM not found.
AMU: *** exit (1) ***


MUSBDriver (mixed.RiscOS.Sources.HWSupport.USB.Controllers.MUSBDriver)...
amu -E  -k rom COMPONENT=MUSBDriver TARGET=MUSBDriver
cc -zM -zps1 -ff -wp -wc -c -depend !Depend   -DKERNEL -D_KERNEL -Dpaddr_t=int -D__P(A)=A
-DKLD_MODULE -DDISABLE_PACKED  -Itbox:,TCPIPLibs:,^.^.NetBSD.,OS: -ff -fah -o o.tps c.tps
Norcroft RISC OS ARM C vsn 5.69 [20 Oct 2010]
cc -zM -zps1 -ff -wp -wc -c -depend !Depend   -DKERNEL -D_KERNEL -Dpaddr_t=int -D__P(A)=A
-DKLD_MODULE -DDISABLE_PACKED  -Itbox:,TCPIPLibs:,^.^.NetBSD.,OS: -ff -fah -o o.musb_util
c.musb_util
Norcroft RISC OS ARM C vsn 5.69 [20 Oct 2010]
cc -zM -zps1 -ff -wp -wc -c -depend !Depend   -DKERNEL -D_KERNEL -Dpaddr_t=int -D__P(A)=A
-DKLD_MODULE -DDISABLE_PACKED  -Itbox:,TCPIPLibs:,^.^.NetBSD.,OS: -ff -fah -o o.musb_usb
c.musb_usb
Norcroft RISC OS ARM C vsn 5.69 [20 Oct 2010]
cc -zM -zps1 -ff -wp -wc -c -depend !Depend   -DKERNEL -D_KERNEL -Dpaddr_t=int -D__P(A)=A
-DKLD_MODULE -DDISABLE_PACKED  -Itbox:,TCPIPLibs:,^.^.NetBSD.,OS: -ff -fah -o o.musb_root
c.musb_root
Norcroft RISC OS ARM C vsn 5.69 [20 Oct 2010]
cc -zM -zps1 -ff -wp -wc -c -depend !Depend   -DKERNEL -D_KERNEL -Dpaddr_t=int -D__P(A)=A
-DKLD_MODULE -DDISABLE_PACKED  -Itbox:,TCPIPLibs:,^.^.NetBSD.,OS: -ff -fah -o o.musb_peri
c.musb_peri
Norcroft RISC OS ARM C vsn 5.69 [20 Oct 2010]
cc -zM -zps1 -ff -wp -wc -c -depend !Depend   -DKERNEL -D_KERNEL -Dpaddr_t=int -D__P(A)=A
```

```
-DKLD_MODULE -DDISABLE_PACKED  -Itbox:,TCPIPLibs:,^.^.NetBSD.,OS: -ff -fah -o o.musb_debug
c.musb_debug
Norcroft RISC OS ARM C vsn 5.69 [20 Oct 2010]
cc -zM -zps1 -ff -wp -wc -c -depend !Depend   -DKERNEL -D_KERNEL -Dpaddr_t=int -D__P(A)=A
-DKLD_MODULE -DDISABLE_PACKED  -Itbox:,TCPIPLibs:,^.^.NetBSD.,OS: -ff -fah -o o.musb
c.musb
Norcroft RISC OS ARM C vsn 5.69 [20 Oct 2010]
cc -zM -zps1 -ff -wp -wc -c -depend !Depend   -DKERNEL -D_KERNEL -Dpaddr_t=int -D__P(A)=A
-DKLD_MODULE -DDISABLE_PACKED  -Itbox:,TCPIPLibs:,^.^.NetBSD.,OS: -ff -fah -o o.cmodule
c.cmodule
Norcroft RISC OS ARM C vsn 5.69 [20 Oct 2010]
"c.cmodule", line 166: Warning: Old-style function 'init_driver'
"c.cmodule", line 189: Warning: Old-style function 'shutdown_driver'
c.cmodule: 2 warnings, 0 errors, 0 serious errors
link -o aof.MUSBDriver -aof o.cmodule o.call_veneer o.musb o.musb_debug o.musb_peri
o.musb_root o.musb_usb o.musb_util o.port o.triggercbs o.tps o.modhead
C:DebugLib.o.DebugLibZM C:ModMalloc.o.Lib_M C:Wild.o.Wild_M C:DDTLib.o.DDTLib_M
C:Desk.o.Desk_M TCPIPLibs:o.unixlibzm TCPIPLibs:o.inetlibzm TCPIPLibs:o.socklib5zm
C:callx.o.callx C:AsmUtils.o.AsmUtilsZM C:tboxlibs.o.eventlibm C:tboxlibs.o.toolboxlib
C:tboxlibs.o.renderlib C:tboxlibs.o.wimplib RISCOSLIB:o.romcstubs
ARM Linker: (Fatal) File C:AsmUtils.o.AsmUtilsZM not found.
AMU: *** exit (1) ***


DisplayManager (castle.RiscOS.Sources.Video.UserI.Display)...
amu -E  -k rom COMPONENT=DisplayManager TARGET=Display
DisplayManager: rom module built

DMAManager (castle.RiscOS.Sources.HWSupport.DMA)...
amu -E  -k rom COMPONENT=DMAManager TARGET=DMA
DMAManager: rom module built

DragASprite (castle.RiscOS.Sources.Desktop.DragASprit)...
amu -E  -k rom COMPONENT=DragASprite TARGET=DragASprit
DragASprite: rom module built

DragAnObj (castle.RiscOS.Sources.Desktop.DragAnObj)...
amu -E  -k rom COMPONENT=DragAnObj TARGET=DragAnObj
DragAnObj: rom module built

DrawMod (castle.RiscOS.Sources.Video.Render.Draw)...
amu -E  -k rom COMPONENT=DrawMod TARGET=DrawMod
DrawMod: rom module built

BBCEconet (castle.RiscOS.Sources.Networking.BBCEconet)...
amu -E  -k rom COMPONENT=BBCEconet TARGET=BBCEconet
BBCEconet: rom module built

FileCore (castle.RiscOS.Sources.FileSys.FileCore)...
amu -E  -k rom COMPONENT=FileCore TARGET=FileCore
FileCore: rom module built

RamFS (castle.RiscOS.Sources.FileSys.RAMFS.RAMFS)...
amu -E  -k rom COMPONENT=RamFS TARGET=RAMFS
RAMFS: rom module built

Filer (castle.RiscOS.Sources.Desktop.Filer)...
amu -E  -k rom COMPONENT=Filer TARGET=Filer
Filer: rom module built
```

```
FilerSWIs (castle.RiscOS.Sources.Desktop.FilerSWIs)...
amu -E  -k rom COMPONENT=FilerSWIs TARGET=FilerSWIs
FilerSWIs: rom module built

FSLock (castle.RiscOS.Sources.FileSys.FSLock)...
amu -E  -k rom COMPONENT=FSLock TARGET=FSLock
AMU: warning - Hard coded SWI XOS_SynchroniseCodeAreas
FSLock: rom module built

FontManager (castle.RiscOS.Sources.Video.Render.Fonts.Manager)...
amu -E  -k rom COMPONENT=FontManager TARGET=Fonts
FontManager: rom module built

FPEmulator (mixed.RiscOS.Sources.HWSupport.FPASC.riscos)...
amu -E  -k rom COMPONENT=FPEmulator TARGET=FPEmulator FPE_APCS=3/32bit System=Iyonix
ObjAsm -I Hdr:t.^ -depend !Depend -APCS 3/32bit -PD "FPEAnchorType SETS \"Low\""
s.CortexA8 o.fpe_rom
ARM AOF Macro Assembler 3.32 (Acorn Computers Ltd) [20 May 2010]
Unrecognised APCS qualifier /fpe3
Target cpu not recognised
Warning: Instruction not supported on targeted CPU at line 143 in file
^.coresrc.^.vensrc.riscos.start
 included by GET/INCLUDE directive at line 76 in file "^.coresrc.s.main"
  143 00000124         MRS     r11, CPSR
Warning: Instruction not supported on targeted CPU at line 164 in file
^.coresrc.^.vensrc.riscos.start
 included by GET/INCLUDE directive at line 76 in file "^.coresrc.s.main"
  164 0000014c         MRS     r11, CPSR
Warning: Instruction not supported on targeted CPU at line 180 in file
^.coresrc.^.vensrc.riscos.start
 included by GET/INCLUDE directive at line 76 in file "^.coresrc.s.main"
  180 00000174         MRS     r11, CPSR
Warning: Instruction not supported on targeted CPU at line 200 in file
^.coresrc.^.vensrc.riscos.start
 included by GET/INCLUDE directive at line 76 in file "^.coresrc.s.main"
  200 000001a8         MRS     r11, CPSR
Warning: Instruction not supported on targeted CPU at line 209 in file
^.coresrc.^.vensrc.riscos.start
 included by GET/INCLUDE directive at line 76 in file "^.coresrc.s.main"
  209 000001bc         MRS     r11, CPSR
Warning: Instruction not supported on targeted CPU at line 228 in file
^.coresrc.^.vensrc.riscos.start
 included by GET/INCLUDE directive at line 76 in file "^.coresrc.s.main"
  228 000001e4         MRS     r11, CPSR
Warning: Instruction not supported on targeted CPU at line 368 in file
^.coresrc.^.vensrc.riscos.start
 included by GET/INCLUDE directive at line 76 in file "^.coresrc.s.main"
  368 00000304         MRS     r0, CPSR
Warning: Instruction not supported on targeted CPU at line 392 in file
^.coresrc.^.vensrc.riscos.start
 included by GET/INCLUDE directive at line 76 in file "^.coresrc.s.main"
  392 00000328         MRS     r3, CPSR                ; interrupts off until
Warning: Instruction not supported on targeted CPU at line 394 in file
^.coresrc.^.vensrc.riscos.start
 included by GET/INCLUDE directive at line 76 in file "^.coresrc.s.main"
  394 00000330         MSR     CPSR_c, r0
Warning: Instruction not supported on targeted CPU at line 412 in file
^.coresrc.^.vensrc.riscos.start
 included by GET/INCLUDE directive at line 76 in file "^.coresrc.s.main"
  412 00000350         MSR     CPSR_c, r3              ; interrupts back on
```

```
Warning: Instruction not supported on targeted CPU at line 101 in file
^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  101 0000042c           MRS     Rwp,CPSR              ;Using Rwp as a temporary
Warning: Instruction not supported on targeted CPU at line 102 in file
^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  102 00000430           MRS     Rtmp2,SPSR
Warning: Instruction not supported on targeted CPU at line 748 in macro InterruptEnable
 at line 183 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  748 0000047c       MRS     Rtmp,CPSR
Warning: Instruction not supported on targeted CPU at line 750 in macro InterruptEnable
 at line 183 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  750 00000484             MSR     CPSR_c,Rtmp
Warning: Instruction not supported on targeted CPU at line 694 in macro Return
 at line 601 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  694 000005b4           MSR     CPSR_csxf,Rtmp2       ; (restoring the CPSR re-disables
Warning: Instruction not supported on targeted CPU at line 695 in macro Return
 at line 601 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  695 000005b8           MSR     SPSR_csxf,Rtmp        ; interrupts, so the SPSR isn't
ever
Warning: Instruction not supported on targeted CPU at line 694 in macro Return
 at line 668 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  694 00000634           MSR     CPSR_csxf,Rtmp2       ; (restoring the CPSR re-disables
Warning: Instruction not supported on targeted CPU at line 695 in macro Return
 at line 668 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  695 00000638           MSR     SPSR_csxf,Rtmp        ; interrupts, so the SPSR isn't
ever
Warning: Instruction not supported on targeted CPU at line 416 in macro
FPE_UseOtherModeAddress
 at line 673 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  416 00000660           MRS     Rtmp2,CPSR                    ;Rtmp2 := original mode
Warning: Instruction not supported on targeted CPU at line 422 in macro
FPE_UseOtherModeAddress
 at line 673 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  422 00000670           MSR     CPSR_c,Rtmp                   ;Change to mode just
calculated
Warning: Instruction not supported on targeted CPU at line 450 in macro
FPE_UseOtherModeAddress
 at line 673 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
```

```
  450 000006ac           MSR     CPSR_c,Rtmp2               ;Change back to original mode
Warning: Instruction not supported on targeted CPU at line 694 in macro Return
 at line 749 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  694 00000780           MSR     CPSR_csxf,Rtmp2       ; (restoring the CPSR re-disables
Warning: Instruction not supported on targeted CPU at line 695 in macro Return
 at line 749 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  695 00000784           MSR     SPSR_csxf,Rtmp        ; interrupts, so the SPSR isn't
ever
Warning: Instruction not supported on targeted CPU at line 416 in macro
FPE_UseOtherModeAddress
 at line 777 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  416 000007f4           MRS     Rtmp2,CPSR                 ;Rtmp2 := original mode
Warning: Instruction not supported on targeted CPU at line 422 in macro
FPE_UseOtherModeAddress
 at line 777 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  422 00000804           MSR     CPSR_c,Rtmp                ;Change to mode just
calculated
Warning: Instruction not supported on targeted CPU at line 450 in macro
FPE_UseOtherModeAddress
 at line 777 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  450 00000840           MSR     CPSR_c,Rtmp2               ;Change back to original mode
Warning: Instruction not supported on targeted CPU at line 694 in macro Return
 at line 857 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  694 00000924           MSR     CPSR_csxf,Rtmp2       ; (restoring the CPSR re-disables
Warning: Instruction not supported on targeted CPU at line 695 in macro Return
 at line 857 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  695 00000928           MSR     SPSR_csxf,Rtmp        ; interrupts, so the SPSR isn't
ever
Warning: Instruction not supported on targeted CPU at line 416 in macro
FPE_UseOtherModeAddress
 at line 886 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  416 000009a0           MRS     Rtmp2,CPSR                 ;Rtmp2 := original mode
Warning: Instruction not supported on targeted CPU at line 422 in macro
FPE_UseOtherModeAddress
 at line 886 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  422 000009b0           MSR     CPSR_c,Rtmp                ;Change to mode just
calculated
Warning: Instruction not supported on targeted CPU at line 450 in macro
FPE_UseOtherModeAddress
 at line 886 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
```

```
  450 000009ec           MSR     CPSR_c,Rtmp2               ;Change back to original mode
Warning: Instruction not supported on targeted CPU at line 416 in macro
FPE_UseOtherModeAddress
 at line 962 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  416 00000b28           MRS     Rtmp2,CPSR                 ;Rtmp2 := original mode
Warning: Instruction not supported on targeted CPU at line 422 in macro
FPE_UseOtherModeAddress
 at line 962 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  422 00000b38           MSR     CPSR_c,Rtmp                ;Change to mode just
calculated
Warning: Instruction not supported on targeted CPU at line 450 in macro
FPE_UseOtherModeAddress
 at line 962 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  450 00000b74           MSR     CPSR_c,Rtmp2               ;Change back to original mode
Warning: Instruction not supported on targeted CPU at line 694 in macro Return
 at line 1088 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  694 00000c80           MSR     CPSR_csxf,Rtmp2       ; (restoring the CPSR re-disables
Warning: Instruction not supported on targeted CPU at line 695 in macro Return
 at line 1088 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  695 00000c84           MSR     SPSR_csxf,Rtmp        ; interrupts, so the SPSR isn't
ever
Warning: Instruction not supported on targeted CPU at line 694 in macro Return
 at line 1181 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  694 00000d1c           MSR     CPSR_csxf,Rtmp2       ; (restoring the CPSR re-disables
Warning: Instruction not supported on targeted CPU at line 695 in macro Return
 at line 1181 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  695 00000d20           MSR     SPSR_csxf,Rtmp        ; interrupts, so the SPSR isn't
ever
Warning: Instruction not supported on targeted CPU at line 482 in macro
FPE_LoadFromOtherModeAddress
 at line 1185 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  482 00000d48           MRS     Rtmp2,CPSR                 ;Rtmp2 := original mode
Warning: Instruction not supported on targeted CPU at line 488 in macro
FPE_LoadFromOtherModeAddress
 at line 1185 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  488 00000d58           MSR     CPSR_c,Rtmp                ;Change to mode just
calculated
Warning: Instruction not supported on targeted CPU at line 537 in macro
FPE_LoadFromOtherModeAddress
 at line 1185 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
```

```
  537 00000d98           MSR     CPSR_c,Rtmp2               ;Change back to original mode
Warning: Instruction not supported on targeted CPU at line 694 in macro Return
 at line 1294 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  694 00000e6c           MSR     CPSR_csxf,Rtmp2       ; (restoring the CPSR re-disables
Warning: Instruction not supported on targeted CPU at line 695 in macro Return
 at line 1294 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  695 00000e70           MSR     SPSR_csxf,Rtmp        ; interrupts, so the SPSR isn't
ever
Warning: Instruction not supported on targeted CPU at line 694 in macro Return
 at line 1389 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  694 00000f14           MSR     CPSR_csxf,Rtmp2       ; (restoring the CPSR re-disables
Warning: Instruction not supported on targeted CPU at line 695 in macro Return
 at line 1389 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  695 00000f18           MSR     SPSR_csxf,Rtmp        ; interrupts, so the SPSR isn't
ever
Warning: Instruction not supported on targeted CPU at line 482 in macro
FPE_LoadFromOtherModeAddress
 at line 1393 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  482 00000f40           MRS     Rtmp2,CPSR                 ;Rtmp2 := original mode
Warning: Instruction not supported on targeted CPU at line 488 in macro
FPE_LoadFromOtherModeAddress
 at line 1393 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  488 00000f50           MSR     CPSR_c,Rtmp                ;Change to mode just
calculated
Warning: Instruction not supported on targeted CPU at line 537 in macro
FPE_LoadFromOtherModeAddress
 at line 1393 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  537 00000f90           MSR     CPSR_c,Rtmp2               ;Change back to original mode
Warning: Instruction not supported on targeted CPU at line 694 in macro Return
 at line 1494 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  694 0000105c           MSR     CPSR_csxf,Rtmp2       ; (restoring the CPSR re-disables
Warning: Instruction not supported on targeted CPU at line 695 in macro Return
 at line 1494 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  695 00001060           MSR     SPSR_csxf,Rtmp        ; interrupts, so the SPSR isn't
ever
Warning: Instruction not supported on targeted CPU at line 694 in macro Return
 at line 1580 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  694 000010f8           MSR     CPSR_csxf,Rtmp2       ; (restoring the CPSR re-disables
Warning: Instruction not supported on targeted CPU at line 695 in macro Return
 at line 1580 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
```

```
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  695 000010fc           MSR     SPSR_csxf,Rtmp        ; interrupts, so the SPSR isn't
ever
Warning: Instruction not supported on targeted CPU at line 482 in macro
FPE_LoadFromOtherModeAddress
 at line 1584 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  482 00001124           MRS     Rtmp2,CPSR                    ;Rtmp2 := original mode
Warning: Instruction not supported on targeted CPU at line 488 in macro
FPE_LoadFromOtherModeAddress
 at line 1584 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  488 00001134           MSR     CPSR_c,Rtmp                   ;Change to mode just
calculated
Warning: Instruction not supported on targeted CPU at line 537 in macro
FPE_LoadFromOtherModeAddress
 at line 1584 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  537 00001174           MSR     CPSR_c,Rtmp2                ;Change back to original mode
Warning: Instruction not supported on targeted CPU at line 482 in macro
FPE_LoadFromOtherModeAddress
 at line 1660 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  482 00001258           MRS     Rtmp2,CPSR                    ;Rtmp2 := original mode
Warning: Instruction not supported on targeted CPU at line 488 in macro
FPE_LoadFromOtherModeAddress
 at line 1660 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  488 00001268           MSR     CPSR_c,Rtmp                   ;Change to mode just
calculated
Warning: Instruction not supported on targeted CPU at line 537 in macro
FPE_LoadFromOtherModeAddress
 at line 1660 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  537 000012b0           MSR     CPSR_c,Rtmp2                ;Change back to original mode
Warning: Instruction not supported on targeted CPU at line 694 in macro Return
 at line 1827 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  694 00001384           MSR     CPSR_csxf,Rtmp2       ; (restoring the CPSR re-disables
Warning: Instruction not supported on targeted CPU at line 695 in macro Return
 at line 1827 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  695 00001388           MSR     SPSR_csxf,Rtmp        ; interrupts, so the SPSR isn't
ever
Warning: Instruction not supported on targeted CPU at line 2178 in file
^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 2178 00001664           MRS     Rtmp2,CPSR                    ; and ensure interrupts
become
Warning: Instruction not supported on targeted CPU at line 2181 in file
```

```
^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 2181 00001670           MSR     CPSR_c,Rtmp                   ;Change to mode just
calculated
Warning: Instruction not supported on targeted CPU at line 2185 in file
^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 2185 00001680           MSR     CPSR_c,Rtmp2                ;Change back to original mode
Warning: Instruction not supported on targeted CPU at line 2250 in file
^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 2250 000016bc           MRS     Rtmp2,CPSR                    ; and ensure interrupts
become
Warning: Instruction not supported on targeted CPU at line 2253 in file
^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 2253 000016c8           MSR     CPSR_c,Rtmp                   ;Change to mode just
calculated
Warning: Instruction not supported on targeted CPU at line 2257 in file
^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 2257 000016d8           MSR     CPSR_c,Rtmp2                  ;Change back to original
mode
Warning: Instruction not supported on targeted CPU at line 2394 in file
^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 2394 0000174c           MRS     Rtmp2,CPSR                    ; and ensure interrupts
become
Warning: Instruction not supported on targeted CPU at line 2397 in file
^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 2397 00001758           MSR     CPSR_c,Rtmp                   ;Change to mode just
calculated
Warning: Instruction not supported on targeted CPU at line 2401 in file
^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 2401 00001768           MSR     CPSR_c,Rtmp2                  ;Change back to original
mode
Warning: Instruction not supported on targeted CPU at line 748 in macro InterruptEnable
 at line 2499 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  748 000017a0       MRS     Rtmp,CPSR
Warning: Instruction not supported on targeted CPU at line 750 in macro InterruptEnable
 at line 2499 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  750 000017a8             MSR     CPSR_c,Rtmp
Warning: Instruction not supported on targeted CPU at line 416 in macro
FPE_UseOtherModeAddress
 at line 2652 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
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 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  416 000018c8           MRS     Rtmp2,CPSR                    ;Rtmp2 := original mode
Warning: Instruction not supported on targeted CPU at line 422 in macro
FPE_UseOtherModeAddress
 at line 2652 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  422 000018d8           MSR     CPSR_c,Rtmp                   ;Change to mode just
calculated
Warning: Instruction not supported on targeted CPU at line 450 in macro
FPE_UseOtherModeAddress
 at line 2652 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  450 00001914           MSR     CPSR_c,Rtmp2                ;Change back to original mode
Warning: Instruction not supported on targeted CPU at line 416 in macro
FPE_UseOtherModeAddress
 at line 2832 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  416 00001a5c           MRS     Rtmp2,CPSR                    ;Rtmp2 := original mode
Warning: Instruction not supported on targeted CPU at line 422 in macro
FPE_UseOtherModeAddress
 at line 2832 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  422 00001a6c           MSR     CPSR_c,Rtmp                   ;Change to mode just
calculated
Warning: Instruction not supported on targeted CPU at line 450 in macro
FPE_UseOtherModeAddress
 at line 2832 in file ^.coresrc.^.coresrc.^.coresrc.s.fpeundef
 included by GET/INCLUDE directive at line 446 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  450 00001aa8           MSR     CPSR_c,Rtmp2                ;Change back to original mode
Warning: Instruction not supported on targeted CPU at line 466 in file
^.coresrc.^.coresrc.s.toplevel
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  466 00001b94             MSR     CPSR_csxf,Rtmp2     ; order must be right: interrupts
Warning: Instruction not supported on targeted CPU at line 467 in file
^.coresrc.^.coresrc.s.toplevel
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  467 00001b98             MSR     SPSR_csxf,Rtmp      ; re-disabled before SPSR valid)
Warning: Instruction not supported on targeted CPU at line 1298 in file
^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 1298 000020a8         MUL     Rtmp2,Rarith,Rtmp2            ;Multiply Rarith by
constant
Warning: Instruction not supported on targeted CPU at line 770 in macro InterruptDisable
 at line 815 in macro EnterRecursive
 at line 1324 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  770 000020cc       MRS     Rtmp2,CPSR
Warning: Instruction not supported on targeted CPU at line 772 in macro InterruptDisable
 at line 815 in macro EnterRecursive
 at line 1324 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  772 000020d4             MSR     CPSR_c,Rtmp2
```

```
Error: Unknown opcode at line 823 in macro EnterRecursive
 at line 1324 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  823 000020e4           WFS     Rtmp2
Error: Unknown opcode at line 827 in macro EnterRecursive
 at line 1324 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  827 000020e8           SFM     F0,(2),[Rtmp2,#-12*(2)]
Error: Unknown opcode at line 1326 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 1326 000020ec         LFM     F0,1,[Rtmp2]
Error: Unknown opcode at line 1338 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 1338 000020fc         LDFE    F1,[Rtmp2]
Error: Unknown opcode at line 1345 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 1345 00002100         DVFPLE  F0,F0,F1
Error: Unknown opcode at line 1346 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 1346 00002100         MUFMIE  F0,F0,F1
Error: Unknown opcode at line 1351 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 1351 00002100         RFS     Rtmp                            ;Make exactness indicator
Error: Unknown opcode at line 855 in macro ExitRecursive
 at line 1357 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  855 00002108           SFM     F0,1,[Rtmp2]
Error: Unknown opcode at line 859 in macro ExitRecursive
 at line 1357 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  859 0000210c           LFM     F0,(2),[Rtmp2,#-12*(2)]
Warning: Instruction not supported on targeted CPU at line 748 in macro InterruptEnable
 at line 865 in macro ExitRecursive
 at line 1357 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  748 00002110       MRS     Rtmp2,CPSR
Warning: Instruction not supported on targeted CPU at line 750 in macro InterruptEnable
 at line 865 in macro ExitRecursive
 at line 1357 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  750 00002118             MSR     CPSR_c,Rtmp2
Error: Unknown opcode at line 1741 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 1741 00002388         DVFPLE  F0,F0,F1                        ; 10^(Rtmp/2, rounded down)
Error: Unknown opcode at line 1742 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 1742 00002388         MUFMIE  F0,F0,F1
```

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Error: Unknown opcode at line 1748 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 1748 0000238c         MUFNEE  F1,F1,#10                       ; 10^(Rtmp/2, rounded up)
Error: Unknown opcode at line 1831 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 1831 00002574         LDFE    F1,[OP1mlo]
Error: Unknown opcode at line 1837 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 1837 0000257c         MUFE    F1,F1,F1                        ;Square result so far
Error: Unknown opcode at line 1840 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 1840 00002584         MUFCSE  F1,F1,#10                       ;Multiply by 10 if bit is 1
Warning: Instruction not supported on targeted CPU at line 770 in macro InterruptDisable
 at line 815 in macro EnterRecursive
 at line 2022 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  770 0000269c       MRS     Rtmp2,CPSR
Warning: Instruction not supported on targeted CPU at line 772 in macro InterruptDisable
 at line 815 in macro EnterRecursive
 at line 2022 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  772 000026a4             MSR     CPSR_c,Rtmp2
Error: Unknown opcode at line 823 in macro EnterRecursive
 at line 2022 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  823 000026b4           WFS     Rtmp2
Error: Unknown opcode at line 827 in macro EnterRecursive
 at line 2022 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  827 000026b8           SFM     F0,(3),[Rtmp2,#-12*(3)]
Error: Unknown opcode at line 2026 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 2026 000026bc         LFM     F0,1,[Rtmp2]
Error: Unknown opcode at line 2031 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 2031 000026c0         RFSNE   Rtmp2
Error: Unknown opcode at line 2033 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 2033 000026c4         WFSNE   Rtmp2
Error: Unknown opcode at line 2124 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 2124 000026e4         LDFLTE  F1,[Rtmp]
Error: Unknown opcode at line 2127 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 2127 000026e8         MUFE    F0,F0,F1
Error: Unknown opcode at line 2148 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
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 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 2148 00002704         LDFLTE  F1,[Rtmp]
Error: Unknown opcode at line 2151 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 2151 00002708         DVFE    F0,F0,F1
Error: Unknown opcode at line 2158 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 2158 00002708         RFS     Rtmp
Error: Unknown opcode at line 855 in macro ExitRecursive
 at line 2164 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  855 00002710           SFM     F0,1,[Rtmp2]
Error: Unknown opcode at line 859 in macro ExitRecursive
 at line 2164 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  859 00002714           LFM     F0,(3),[Rtmp2,#-12*(3)]
Warning: Instruction not supported on targeted CPU at line 748 in macro InterruptEnable
 at line 865 in macro ExitRecursive
 at line 2164 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  748 00002718       MRS     Rtmp2,CPSR
Warning: Instruction not supported on targeted CPU at line 750 in macro InterruptEnable
 at line 865 in macro ExitRecursive
 at line 2164 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  750 00002720             MSR     CPSR_c,Rtmp2
Error: Unknown opcode at line 2193 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 2193 00002758         LFM     F2,1,[Rtmp2]
Error: Unknown opcode at line 2194 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 2194 00002758         MUFE    F0,F0,F2
Error: Unknown opcode at line 2198 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 2198 00002758         MUFE    F0,F0,F1
Error: Unknown opcode at line 2200 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 2200 0000275c         MUFNEE  F1,F1,#10
Error: Unknown opcode at line 2201 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 2201 0000275c         MUFE    F1,F0,F1
Error: Unknown opcode at line 2206 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 2206 00002760         LFM     F0,1,[Rtmp2]
Error: Unknown opcode at line 2207 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 2207 00002760         MUFE    F0,F1,F0
```

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Error: Unknown opcode at line 2212 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 2212 00002760         RFS     Rtmp2
Error: Unknown opcode at line 2216 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 2216 00002768         MUFE    F0,F1,F2
Error: Unknown opcode at line 2224 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 2224 00002768         RFS     Rtmp
Error: Unknown opcode at line 855 in macro ExitRecursive
 at line 2230 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  855 00002770           SFM     F0,1,[Rtmp2]
Error: Unknown opcode at line 859 in macro ExitRecursive
 at line 2230 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  859 00002774           LFM     F0,(3),[Rtmp2,#-12*(3)]
Warning: Instruction not supported on targeted CPU at line 748 in macro InterruptEnable
 at line 865 in macro ExitRecursive
 at line 2230 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  748 00002778       MRS     Rtmp2,CPSR
Warning: Instruction not supported on targeted CPU at line 750 in macro InterruptEnable
 at line 865 in macro ExitRecursive
 at line 2230 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  750 00002780             MSR     CPSR_c,Rtmp2
Error: Unknown opcode at line 2268 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 2268 000027d4         LFM     F2,1,[Rtmp2]
Error: Unknown opcode at line 2269 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 2269 000027d4         MUFE    F0,F0,F2
Error: Unknown opcode at line 2275 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 2275 000027d4         MUFE    F0,F0,F1
Error: Unknown opcode at line 2276 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 2276 000027d4         MUFE    F0,F0,F1
Error: Unknown opcode at line 2277 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 2277 000027d4         MUFE    F0,F0,F2
Error: Unknown opcode at line 2279 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 2279 000027d8         MUFNEE  F1,F1,#10
Error: Unknown opcode at line 2280 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
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 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 2280 000027d8         MUFE    F0,F0,F1
Error: Unknown opcode at line 2282 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 2282 000027dc         MUFNEE  F1,F1,#10
Error: Unknown opcode at line 2283 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 2283 000027dc         MUFE    F0,F0,F1
Error: Unknown opcode at line 2288 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 2288 000027dc         RFS     Rtmp2
Error: Unknown opcode at line 2295 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
 2295 000027e8         SFM     F0,1,[Rtmp2]
Error: Unknown opcode at line 859 in macro ExitRecursive
 at line 2302 in file ^.coresrc.^.coresrc.^.coresrc.s.ldst
 included by GET/INCLUDE directive at line 565 in file "^.coresrc.^.coresrc.s.toplevel"
 included by GET/INCLUDE directive at line 77 in file "^.coresrc.s.main"
  859 000027f0           LFM     F0,(3),[Rtmp2,#-12*(3)]
Assembly terminated:
51 Errors, 90 Warnings
AMU: *** exit (8) ***


VFPSupport (bsd.RiscOS.Sources.HWSupport.VFPSupport)...
amu -E  -k rom COMPONENT=VFPSupport TARGET=VFPSupport
VFPSupport: rom module built

Free (castle.RiscOS.Sources.Desktop.Free)...
amu -E  -k rom COMPONENT=Free TARGET=Free
Free: rom module built

Hourglass (castle.RiscOS.Sources.Video.Render.Hourglass)...
amu -E  -k rom COMPONENT=Hourglass TARGET=Hourglass
Hourglass: rom module built

IIC (castle.RiscOS.Sources.HWSupport.IIC)...
amu -E  -k rom COMPONENT=IIC TARGET=IIC
IIC: rom module built

International (castle.RiscOS.Sources.Internat.Inter)...
amu -E  -k rom COMPONENT=International TARGET=Inter
International: rom module built

InternationalKeyboard (castle.RiscOS.Sources.Internat.IntKey)...
amu -E  -k rom COMPONENT=InternationalKeyboard TARGET=IntKey KEYBOARD=All
InternationalKeyboard: rom module built

ITable (castle.RiscOS.Sources.Video.Render.Fonts.ITable)...
amu -E  -k rom COMPONENT=ITable TARGET=ITable
AMU: Don't know how to make 'C:AsmUtils.o.AsmUtilsZM'

NetFS (castle.RiscOS.Sources.FileSys.NetFS.NetFS)...
amu -E  -k rom COMPONENT=NetFS TARGET=NetFS
NetFS: rom module built
```

```
NetFiler (castle.RiscOS.Sources.FileSys.NetFS.NetFiler)...
amu -E  -k rom COMPONENT=NetFiler TARGET=NetFiler
NetFiler: rom module built

NetPrint (castle.RiscOS.Sources.FileSys.NetPrint)...
amu -E  -k rom COMPONENT=NetPrint TARGET=NetPrint
NetPrint: rom module built

NetStatus (castle.RiscOS.Sources.Networking.NetStatus)...
amu -E  -k rom COMPONENT=NetStatus TARGET=NetStatus
NetStatus: rom module built

NetUtils (castle.RiscOS.Sources.Networking.NetUtils2)...
amu -E  -k rom COMPONENT=NetUtils TARGET=NetUtils2
NetUtils: rom module built

Obey (castle.RiscOS.Sources.Programmer.Obey)...
amu -E  -k rom COMPONENT=Obey TARGET=Obey
Obey: rom module built

Pinboard (castle.RiscOS.Sources.Desktop.Pinboard)...
amu -E  -k rom COMPONENT=Pinboard TARGET=Pinboard
Pinboard: rom module built

PipeFS (castle.RiscOS.Sources.FileSys.PipeFS)...
amu -E  -k rom COMPONENT=PipeFS TARGET=PipeFS
PipeFS: rom module built

RAMFSFiler (castle.RiscOS.Sources.FileSys.RAMFS.RAMFSFiler)...
amu -E  -k rom COMPONENT=RAMFSFiler TARGET=RAMFSFiler
RAMFSFiler: rom module built

ResourceFiler (castle.RiscOS.Sources.FileSys.ResourceFS.ResFiler)...
amu -E  -k rom COMPONENT=ResourceFiler TARGET=ResFiler
ResourceFiler: rom module built

ROMFonts (castle.RiscOS.Sources.Video.Render.Fonts.ROMFonts)...
amu -E  -k rom COMPONENT=ROMFonts TARGET=ROMFonts
ROMFonts: rom module built

ScreenBlanker (castle.RiscOS.Sources.Video.Render.ScrBlank)...
amu -E  -k rom COMPONENT=ScreenBlanker TARGET=ScrBlank
ScreenBlanker: rom module built

ScrSaver (castle.RiscOS.Sources.Video.UserI.ScrSaver)...
amu -E  -k rom COMPONENT=ScrSaver TARGET=ScrSaver SCRSAVERAPP=No
ScrSaver: rom module built

ShellCLI (castle.RiscOS.Sources.Desktop.ShellCLI)...
amu -E  -k rom COMPONENT=ShellCLI TARGET=ShellCLI
ShellCLI: rom module built

SoundDMA_HAL (castle.RiscOS.Sources.HWSupport.Sound.Sound0HAL)...
amu -E  -k rom COMPONENT=SoundDMA_HAL TARGET=Sound0
SoundDMA: rom module built

SoundControl (castle.RiscOS.Sources.Audio.SoundCtrl)...
amu -E  -k rom COMPONENT=SoundControl TARGET=SoundCtrl
SoundCtrl: rom module built
```

```
SoundChannels (castle.RiscOS.Sources.HWSupport.Sound.Sound1)...
amu -E  -k rom COMPONENT=SoundChannels TARGET=Sound1
SoundChannels: rom module built

SoundScheduler (castle.RiscOS.Sources.HWSupport.Sound.Sound2)...
amu -E  -k rom COMPONENT=SoundScheduler TARGET=Sound2
SoundScheduler: rom module built

SpriteExtend (mixed.RiscOS.Sources.Video.Render.SprExtend)...
amu -E  -k rom COMPONENT=SpriteExtend TARGET=SprExtend
SpriteExtend: rom module built

SpriteUtils (castle.RiscOS.Sources.Video.Render.SpriteUtil)...
amu -E  -k rom COMPONENT=SpriteUtils TARGET=SpriteUtil
SpriteUtils: rom module built

Squash (castle.RiscOS.Sources.Programmer.Squash)...
amu -E  -k rom COMPONENT=Squash TARGET=Squash

SuperSample (castle.RiscOS.Sources.Video.Render.Super)...
amu -E  -k rom COMPONENT=SuperSample TARGET=Super
SuperSample: rom module built

SystemDevices (castle.RiscOS.Sources.HWSupport.SystemDevs)...
amu -E  -k rom COMPONENT=SystemDevices TARGET=SystemDevs
SystemDevices: rom module built

TaskWindow (castle.RiscOS.Sources.Desktop.TaskWindow)...
amu -E  -k rom COMPONENT=TaskWindow TARGET=TaskWindow
TaskWindow: rom module built

WindowUtils (castle.RiscOS.Sources.Desktop.WimpUtils)...
amu -E  -k rom COMPONENT=WindowUtils TARGET=WimpUtils2
WindowUtils: rom module built

FilterManager (castle.RiscOS.Sources.Desktop.Filter)...
amu -E  -k rom COMPONENT=FilterManager TARGET=FilterMgr
FilterManager: rom module built

WaveSynth (castle.RiscOS.Sources.HWSupport.Sound.Voices.WaveSynth)...
amu -E  -k rom COMPONENT=WaveSynth TARGET=WaveSynth
WaveSynth: rom module built

StringLib (castle.RiscOS.Sources.HWSupport.Sound.Voices.StringLib)...
amu -E  -k rom COMPONENT=StringLib TARGET=StringLib
StringLib: rom module built

Percussion (castle.RiscOS.Sources.HWSupport.Sound.Voices.Percussion)...
amu -E  -k rom COMPONENT=Percussion TARGET=Percussion
Percussion: rom module built

Filer_Action (castle.RiscOS.Sources.Desktop.FilerAct)...
amu -E  -k rom COMPONENT=Filer_Action TARGET=FilerAct
FilerAct: rom module built

DOSFS (castle.RiscOS.Sources.FileSys.ImageFS.DOSFS)...
amu -E  -k rom COMPONENT=DOSFS TARGET=DOSFS PCMCIA=TRUE
DOSFS: rom module built

SCSISwitch (castle.RiscOS.Sources.HWSupport.SCSI.SCSISwitch)...
```

```
amu -E  -k rom COMPONENT=SCSISwitch TARGET=SCSIDriver
SCSIdriver: rom complete

SCSISoftUSB (mixed.RiscOS.Sources.HWSupport.SCSI.SCSISoftUSB)...
amu -E  -k rom COMPONENT=SCSISoftUSB TARGET=SCSISoftUSB
do mkdir -p gpa
do mkdir -p aif
do mkdir -p do
do mkdir -p o
do mkdir -p aof
link -o aof.SCSISoftUSB -aof o.moduleROM o.svcprint  o.glue  o.umass  o.umass_quirks
o.global o.asm o.modhdr  RISCOSLIB:o.romcstubs
SCSISoftUSB: rom module built

SCSIFS (castle.RiscOS.Sources.FileSys.SCSIFS.SCSIFS)...
amu -E  -k rom COMPONENT=SCSIFS TARGET=SCSIFS
SCSIFS: rom module built

SCSIFiler (castle.RiscOS.Sources.FileSys.ADFS.ADFSFiler)...
amu -E  -k rom COMPONENT=SCSIFiler TARGET=SCSIFiler ASFLAGS="-PD \"SCSI SETL {TRUE}\""
SCSITEMPLATES=yes
SCSIFiler: rom module built

ColourPicker (castle.RiscOS.Sources.Video.UserI.Picker)...
amu -E  -k rom COMPONENT=ColourPicker TARGET=Picker
do mkdir -p aof
link -o aof.Picker -aof or.cmyk  or.dialogue  or.helpreply  or.hsv
or.main  or.model     or.rgb        or.tables
or.callback  or.lookup     or.realloc                              or.task  or.riscos
or.window     or.resource                           or.icon  or.steppable or.relocate
o.veneer o.header OSLib:o.OSLib RISCOSLIB:o.romcstubs C:AsmUtils.o.AsmUtilsZM
ARM Linker: (Fatal) File C:AsmUtils.o.AsmUtilsZM not found.
AMU: *** exit (1) ***


ScreenModes (castle.RiscOS.Sources.Video.UserI.ScrModes)...
amu -E  -k rom COMPONENT=ScreenModes TARGET=ScrModes
ScrModes: rom module built

DrawFile (castle.RiscOS.Sources.Video.Render.DrawFile)...
amu -E  -k rom COMPONENT=DrawFile TARGET=DrawFile
AMU: in makefile Makefile (line 39):
AMU: Re-inclusion of Makefiles:StdTools
AMU: in makefile Makefile (line 40):
AMU: Re-inclusion of Makefiles:DbgRules
AMU: Don't know how to make 'C:AsmUtils.o.AsmUtilsZM'

BootCommands (castle.RiscOS.Sources.Programmer.BootCmds)...
amu -E  -k rom COMPONENT=BootCommands TARGET=BootCmds
BootCmds: rom module built

AUNMsgs (castle.RiscOS.Sources.Networking.AUN.AUNMsgs)...
amu -E  -k rom COMPONENT=AUNMsgs TARGET=AUNMsgs
do <Perl$Dir>.perl build:getversion AUNMsgs$Version
Do modgen rm.AUNMsgs AUNMsgs "AUN Messages" <AUNMsgs$Version> -via Resources.UK.<System>
AUNMsgs: rom module built

MManager (castle.RiscOS.Sources.Networking.AUN.MManager)...
amu -E  -k rom COMPONENT=MManager TARGET=MManager
```

```
Internet (mixed.RiscOS.Sources.Networking.AUN.Internet.build)...
amu -E  -k rom COMPONENT=Internet TARGET=Internet
Internet: Module built (ROM)

Resolver (castle.RiscOS.Sources.Networking.Resolver)...
amu -E  -k rom COMPONENT=Resolver TARGET=Resolver

Net (castle.RiscOS.Sources.Networking.AUN.Net)...
amu -E  -k rom COMPONENT=Net TARGET=Net
link -o aof.Net -aof o.mnshdr_b o.mns o.mnscommon o.io o.swis o.configure o.netasm o.route
o.showrt           o.text o.inetfn o.debug TCPIPLibs:o.unixlibzm TCPIPLibs:o.inetlibzm
TCPIPLibs:o.socklib5zm C:AsmUtils.o.AsmUtilsZM RISCOSLIB:o.romstubs
ARM Linker: (Fatal) File C:AsmUtils.o.AsmUtilsZM not found.
AMU: *** exit (1) ***


BootNet (castle.RiscOS.Sources.Networking.AUN.BootNet)...
amu -E  -k rom COMPONENT=BootNet TARGET=BootNet
BootNet: rom module built

Freeway (castle.RiscOS.Sources.Networking.AUN.Access.Freeway)...
amu -E  -k rom COMPONENT=Freeway TARGET=Freeway
AMU: Don't know how to make 'C:AsmUtils.o.AsmUtilsZM'

ShareFS (castle.RiscOS.Sources.Networking.AUN.Access.ShareFS.ShareFS)...
amu -E  -k rom COMPONENT=ShareFS TARGET=ShareFS

MimeMap (castle.RiscOS.Sources.Networking.MimeMap)...
amu -E  -k rom COMPONENT=MimeMap TARGET=MimeMap

LanManFS (castle.RiscOS.Sources.Networking.Omni.Protocols.LanManFS)...
amu -E  -k rom COMPONENT=LanManFS TARGET=LanManFS OPTIONS=-DCHECK_ARMBOOT_EXISTS
ROMSPRITES=TRUE
do mkdir -p aof
link -o aof.LanManFS -aof LanMan_MH.o Errors.o Interface.o or.LanMan or.Omni or.Logon
or.CoreFn or.Printers or.NameCache or.Xlate or.buflib or.Transact or.LLC or.NetBIOS or.SMB
or.Attr or.RPC or.NBIP or.Stats RISCOSLIB:o.romcstubs TCPIPLibs:o.unixlibzm
TCPIPLibs:o.inetlibzm TCPIPLibs:o.socklibzm C:AsmUtils.o.AsmUtilsZM
ARM Linker: (Fatal) File C:AsmUtils.o.AsmUtilsZM not found.
AMU: *** exit (1) ***


DHCP (castle.RiscOS.Sources.Networking.DHCP)...
amu -E  -k rom COMPONENT=DHCP TARGET=DHCP OPTIONS=-DMINIMUM_OPTIONS_LENGTH=4
AMU: Don't know how to make 'C:AsmUtils.o.AsmUtilsZM'

Edit (castle.RiscOS.Sources.Apps.Edit)...
amu -E  -k rom COMPONENT=Edit TARGET=Edit
Edit: Module built (ROM)

Draw (castle.RiscOS.Sources.Apps.Draw)...
amu -E  -k rom COMPONENT=Draw TARGET=Draw
Draw: Module built (ROM)

Paint (castle.RiscOS.Sources.Apps.Paint)...
amu -E  -k rom COMPONENT=Paint TARGET=Paint
Paint: Module built (ROM)

Alarm (castle.RiscOS.Sources.Apps.Alarm)...
amu -E  -k rom COMPONENT=Alarm TARGET=Alarm
```

```
Alarm: Module built (ROM}

Chars (castle.RiscOS.Sources.Apps.Chars)...
amu -E  -k rom COMPONENT=Chars TARGET=Chars
Chars: Module built (ROM}

Help2 (castle.RiscOS.Sources.Apps.Help2)...
amu -E  -k rom COMPONENT=Help2 TARGET=Help
do <Perl$Dir>.perl build:getversion Help2$BuildVersion
do mkdir -p rm
Do modgen rm.Help !Help "!Help" <Help2$BuildVersion> -via Resources.Filelist
Help: rom module built

tboxlib (castle.RiscOS.Sources.Toolbox.Common)...
amu -E  -k rom COMPONENT=tboxlib

TinyStubs (castle.RiscOS.Sources.Toolbox.TinyStubs)...
amu -E  -k rom COMPONENT=TinyStubs TARGET=TinyStubs
AMU: in makefile Makefile (line 34):
AMU: Re-inclusion of Makefiles:StdTools
AMU: in makefile Makefile (line 35):
AMU: Re-inclusion of Makefiles:DbgRules
TinyStubs: rom module built

Toolbox (castle.RiscOS.Sources.Toolbox.Toolbox)...
amu -E  -k rom COMPONENT=Toolbox TARGET=Toolbox
Toolbox: rom module built

Window (castle.RiscOS.Sources.Toolbox.Window)...
amu -E  -k rom COMPONENT=Window TARGET=Window
Window: rom module built

ToolAction (castle.RiscOS.Sources.Toolbox.ToolAction)...
amu -E  -k rom COMPONENT=ToolAction TARGET=ToolAction
ToolAction: rom module built

Menu (castle.RiscOS.Sources.Toolbox.Menu)...
amu -E  -k rom COMPONENT=Menu TARGET=Menu
Menu: rom module built

IconBar (castle.RiscOS.Sources.Toolbox.IconBar)...
amu -E  -k rom COMPONENT=IconBar TARGET=IconBar
IconBar: rom module built

ColourDbox (castle.RiscOS.Sources.Toolbox.ColourDbox)...
amu -E  -k rom COMPONENT=ColourDbox TARGET=ColourDbox
ColourDbox: rom module built

ColourMenu (castle.RiscOS.Sources.Toolbox.ColourMenu)...
amu -E  -k rom COMPONENT=ColourMenu TARGET=ColourMenu
ColourMenu: rom module built

DCS_Quit (castle.RiscOS.Sources.Toolbox.DCS)...
amu -E  -k rom COMPONENT=DCS_Quit TARGET=DCS
DCS_Quit: rom module built

FileInfo (castle.RiscOS.Sources.Toolbox.FileInfo)...
amu -E  -k rom COMPONENT=FileInfo TARGET=FileInfo
FileInfo: rom module built
```

```
FontDbox (castle.RiscOS.Sources.Toolbox.FontDbox)...
amu -E  -k rom COMPONENT=FontDbox TARGET=FontDbox
FontDbox: rom module built

FontMenu (castle.RiscOS.Sources.Toolbox.FontMenu)...
amu -E  -k rom COMPONENT=FontMenu TARGET=FontMenu
FontMenu: rom module built

PrintDbox (castle.RiscOS.Sources.Toolbox.PrintDbox)...
amu -E  -k rom COMPONENT=PrintDbox TARGET=PrintDbox
PrintDbox: rom module built

ProgInfo (castle.RiscOS.Sources.Toolbox.ProgInfo)...
amu -E  -k rom COMPONENT=ProgInfo TARGET=ProgInfo
ProgInfo: rom module built

SaveAs (castle.RiscOS.Sources.Toolbox.SaveAs)...
amu -E  -k rom COMPONENT=SaveAs TARGET=SaveAs
SaveAs: rom module built

Scale (castle.RiscOS.Sources.Toolbox.Scale)...
amu -E  -k rom COMPONENT=Scale TARGET=Scale
Scale: rom module built

Gadgets (castle.RiscOS.Sources.Toolbox.Gadgets)...
amu -E  -k rom COMPONENT=Gadgets TARGET=TextGadget
TextGadget: Module built (ROM)

CDFSDriver (castle.RiscOS.Sources.HWSupport.CD.CDFSDriver)...
amu -E  -k rom COMPONENT=CDFSDriver TARGET=CDFSDriver
CDFSDriver: rom module built

CDFS (castle.RiscOS.Sources.FileSys.CDFS.CDFS)...
amu -E  -k rom COMPONENT=CDFS TARGET=CDFS
CDFS: rom module built

CDFSFiler (castle.RiscOS.Sources.FileSys.CDFS.CDFSFiler)...
amu -E  -k rom COMPONENT=CDFSFiler TARGET=CDFSFiler
CDFSFiler: rom module built
================================================================================
Starting phase install_rom ...

HAL_OMAP3 (castle.RiscOS.Sources.HAL.OMAP3)...
amu -E  install_rom
INSTDIR=HostFS::HardDisc4.$.Build.temp.OMAP3Dev.Install.ROOL.OMAP3.RISC_OS
COMPONENT=HAL_OMAP3 TARGET=OMAP3
AMU: in makefile included from Makefile (line 37):
AMU: in makefile Makefiles:CModule (line 191):
AMU: Re-inclusion of Makefiles:StdRules
copy  linked.OMAP3
HostFS::HardDisc4.$.Build.temp.OMAP3Dev.Install.ROOL.OMAP3.RISC_OS.OMAP3 FR~C~V~N
OMAP-3 HAL: rom module installed

Kernel (castle.RiscOS.Sources.Kernel)...
amu -E  install_rom
INSTDIR=HostFS::HardDisc4.$.Build.temp.OMAP3Dev.Install.ROOL.OMAP3.RISC_OS
COMPONENT=Kernel TARGET=Kernel
copy rm.Kernel HostFS::HardDisc4.$.Build.temp.OMAP3Dev.Install.ROOL.OMAP3.RISC_OS.Kernel
~cfr~v
Kernel: rom module installed
```

```
PCI (castle.RiscOS.Sources.HWSupport.PCI)...
amu -E  install_rom
INSTDIR=HostFS::HardDisc4.$.Build.temp.OMAP3Dev.Install.ROOL.OMAP3.HWSupport COMPONENT=PCI
TARGET=PCI
copy  rm.CortexA8.PCI
HostFS::HardDisc4.$.Build.temp.OMAP3Dev.Install.ROOL.OMAP3.HWSupport.PCI FR~C~V~N
PCI: rom module installed

FileSwitch (castle.RiscOS.Sources.FileSys.FileSwitch)...
amu -E  install_rom
INSTDIR=HostFS::HardDisc4.$.Build.temp.OMAP3Dev.Install.ROOL.OMAP3.FileSys
COMPONENT=FileSwitch TARGET=FileSwitch
copy  rm.CortexA8.FileSwitch
HostFS::HardDisc4.$.Build.temp.OMAP3Dev.Install.ROOL.OMAP3.FileSys.FileSwitch FR~C~V~N
FileSwitch: rom module installed

ResourceFS (castle.RiscOS.Sources.FileSys.ResourceFS.ResourceFS)...
amu -E  install_rom
INSTDIR=HostFS::HardDisc4.$.Build.temp.OMAP3Dev.Install.ROOL.OMAP3.FileSys
COMPONENT=ResourceFS TARGET=ResourceFS
copy  rm.CortexA8.ResourceFS
HostFS::HardDisc4.$.Build.temp.OMAP3Dev.Install.ROOL.OMAP3.FileSys.ResourceFS FR~C~V~N
ResourceFS: rom module installed

TerritoryManager (castle.RiscOS.Sources.Internat.Territory.Manager)...
amu -E  install_rom
INSTDIR=HostFS::HardDisc4.$.Build.temp.OMAP3Dev.Install.ROOL.OMAP3.Internat
COMPONENT=TerritoryManager TARGET=TerrMgr
copy  rm.CortexA8.TerrMgr
HostFS::HardDisc4.$.Build.temp.OMAP3Dev.Install.ROOL.OMAP3.Internat.TerrMgr FR~C~V~N
TerritoryManager: rom module installed

Messages (castle.RiscOS.Sources.Internat.Messages)...
amu -E  install_rom
INSTDIR=HostFS::HardDisc4.$.Build.temp.OMAP3Dev.Install.ROOL.OMAP3.Internat
COMPONENT=Messages TARGET=Messages
Utils.ScanRes Processed.ROOL.OMAP3.<Build$LocaleListNumeric> Data.ROOL.OMAP3.<Build
$LocaleListNumeric>.Data
Scanning from directory Processed.ROOL.OMAP3.<Build$LocaleListNumeric>
Directory is
HostFS::HardDisc4.$.Build.temp.OMAP3Dev.castle.RiscOS.Sources.Internat.Messages.Processed.
ROOL.OMAP3.01.Common
Country code for Common is 0
Directory 0 is Common (territory numbers: 0 )
Appending data for territory resource dir
HostFS::HardDisc4.$.Build.temp.OMAP3Dev.castle.RiscOS.Sources.Internat.Messages.Processed.
ROOL.OMAP3.01.Common
set resdata Data.ROOL.OMAP3.<Build$LocaleListNumeric>.Data
objasm -Stamp -quit -depend !Depend    -ihdr -i<Hdr$Dir>.Global -i<Hdr$Dir>.Interface -
i<Hdr$Dir>.Interface2 -pd "APCS SETS \"APCS-32\"" -pd "Machine SETS \"CortexA8\"" -pd
"UserIF SETS \"Iyonix\"" -o o.Messages s.Messages
ARM AOF Macro Assembler 3.32 (Acorn Computers Ltd) [20 May 2010]
Unrecognised APCS qualifier /fpe3
Target cpu not recognised
link  -o rm.ROOL.OMAP3.<Build$LocaleListNumeric>.Messages -rmf o.Messages
unset resdata
copy  rm.ROOL.OMAP3.<Build$LocaleListNumeric>.Messages
HostFS::HardDisc4.$.Build.temp.OMAP3Dev.Install.ROOL.OMAP3.Internat.Messages FR~C~V~N
Messages: rom module installed
```

```
MessageTrans (castle.RiscOS.Sources.Internat.MsgTrans)...
amu -E  install_rom
INSTDIR=HostFS::HardDisc4.$.Build.temp.OMAP3Dev.Install.ROOL.OMAP3.Internat
COMPONENT=MessageTrans TARGET=MsgTrans
copy  rm.CortexA8.MsgTrans
HostFS::HardDisc4.$.Build.temp.OMAP3Dev.Install.ROOL.OMAP3.Internat.MsgTrans FR~C~V~N
MessageTrans: rom module installed

UK (castle.RiscOS.Sources.Internat.Territory.Module)...
amu -E  install_rom
INSTDIR=HostFS::HardDisc4.$.Build.temp.OMAP3Dev.Install.ROOL.OMAP3.Internat COMPONENT=UK
TARGET=UK
copy  rm.CortexA8.UK
HostFS::HardDisc4.$.Build.temp.OMAP3Dev.Install.ROOL.OMAP3.Internat.UK FR~C~V~N
UK: rom module installed

WindowManager (castle.RiscOS.Sources.Desktop.Wimp)...
amu -E  install_rom
INSTDIR=HostFS::HardDisc4.$.Build.temp.OMAP3Dev.Install.ROOL.OMAP3.Desktop
COMPONENT=WindowManager TARGET=Wimp OPTIONS=Ursula
do mkdir -p o.CortexA8
objasm -NoWarn -PreDefine "Options SETS \"Ursula\"" -Stamp -quit -depend !Depend    -ihdr
-i<Hdr$Dir>.Global -i<Hdr$Dir>.Interface -i<Hdr$Dir>.Interface2 -pd "APCS SETS
\"APCS-32\"" -pd "Machine SETS \"CortexA8\"" -pd "UserIF SETS \"Iyonix\"" -o
o.CortexA8.Wimp s.Wimp
ARM AOF Macro Assembler 3.32 (Acorn Computers Ltd) [20 May 2010]
Unrecognised APCS qualifier /fpe3
Target cpu not recognised
Error: Unknown opcode at line 1109 in file s.Wimp07
 included by GET/INCLUDE directive at line 103 in file "s.Wimp"
 1109 00014a48         WFSEQ   R5
Error: Unknown opcode at line 1115 in file s.Wimp07
 included by GET/INCLUDE directive at line 103 in file "s.Wimp"
 1115 00014a50         WFS     R5                      ; will still occur if FPEmulator
RMKilled
Error: Unknown opcode at line 1137 in file s.Wimp07
 included by GET/INCLUDE directive at line 103 in file "s.Wimp"
 1137 00014a5c         WFS     R5
Error: Unknown opcode at line 1367 in file s.Wimp07
 included by GET/INCLUDE directive at line 103 in file "s.Wimp"
 1367 00014bb0         RFS     R1                      ; <==== NB: pending trap can occur
here
Error: Unknown opcode at line 1383 in file s.Wimp07
 included by GET/INCLUDE directive at line 103 in file "s.Wimp"
 1383 00014bd8         WFS     R1
Assembly terminated:
5 Errors, 67 Warnings suppressed by -NOWarn
AMU: *** exit (1) ***

AMU: *** 'install_rom' not re-made because of errors ***

Error running make install_rom on module 'WindowManager'.
Fatal error running make install_rom on module 'WindowManager'.
Batched errors...
Error running make install_rom on module 'WindowManager'.
--------------------------------------------------------------------------------
Closing log file 'HostFS::HardDisc4.$.Build.temp.OMAP3Dev.BuildSys.Logs.bUI800-00'.
```